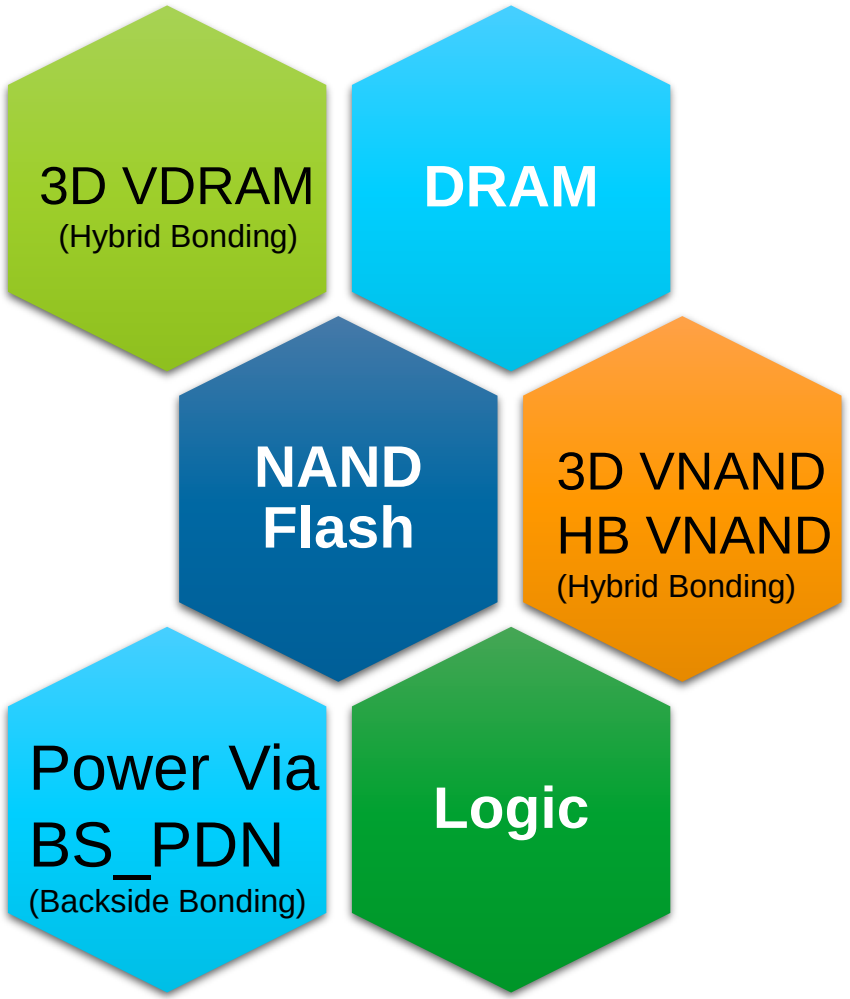
진공기술실무수련회교육

"반도체 최신 기술동향"

한국알박㈜

Outline: 반도체 최신 기술동향

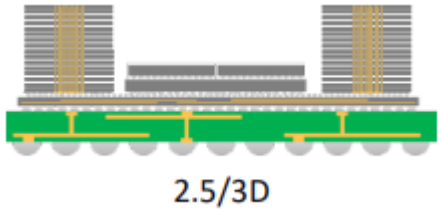


*PDN: Power Distribution Network

「More Moore」 「More than Moore」

Transistor density
Performance
Power efficiency

Advanced Packaging
- 2.5D
- 3D



Patterning
- **EUV**
- **Dry PR** (Photo Resist)
- **ALE** Atomic layer control

Deposition
- **ALD**
- **ASD** Selective deposition

3D stacking
- **Hybrid bonding**

*ALE: Atomic Layer Etching
*ALD: Atomic Layer Deposition
*ASD: Area Selective Deposition

Contents

Introduction : Moore's Law

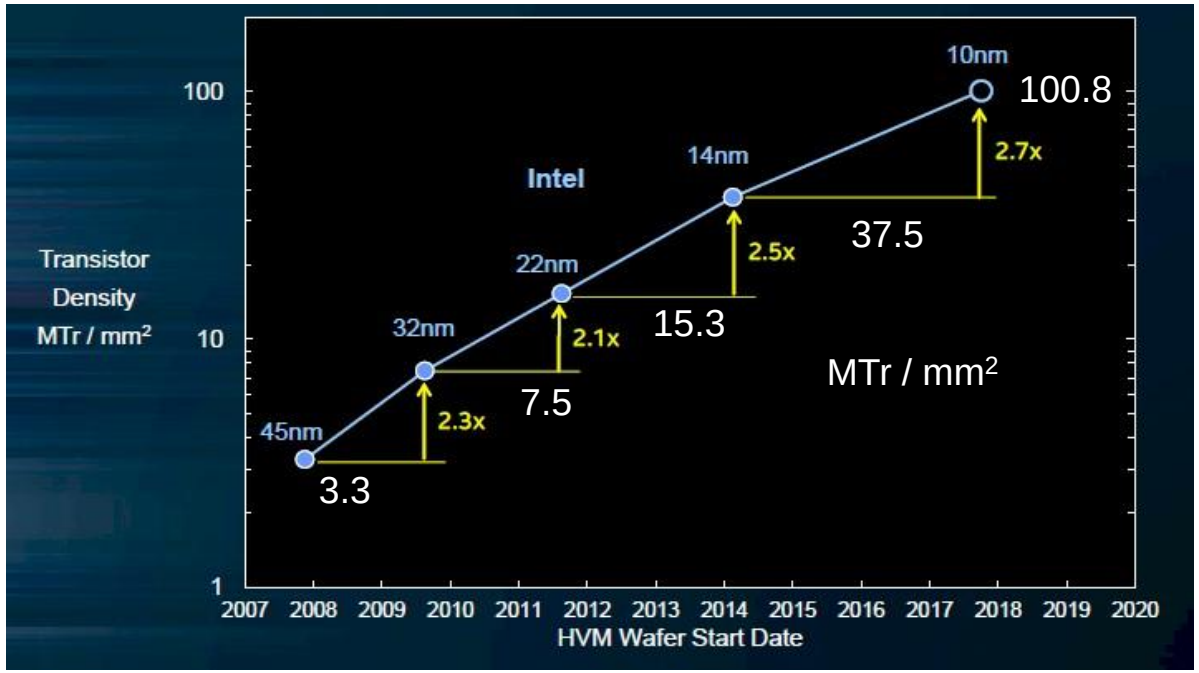
인텔(Intel) - 공동창업주 Gordon Moore

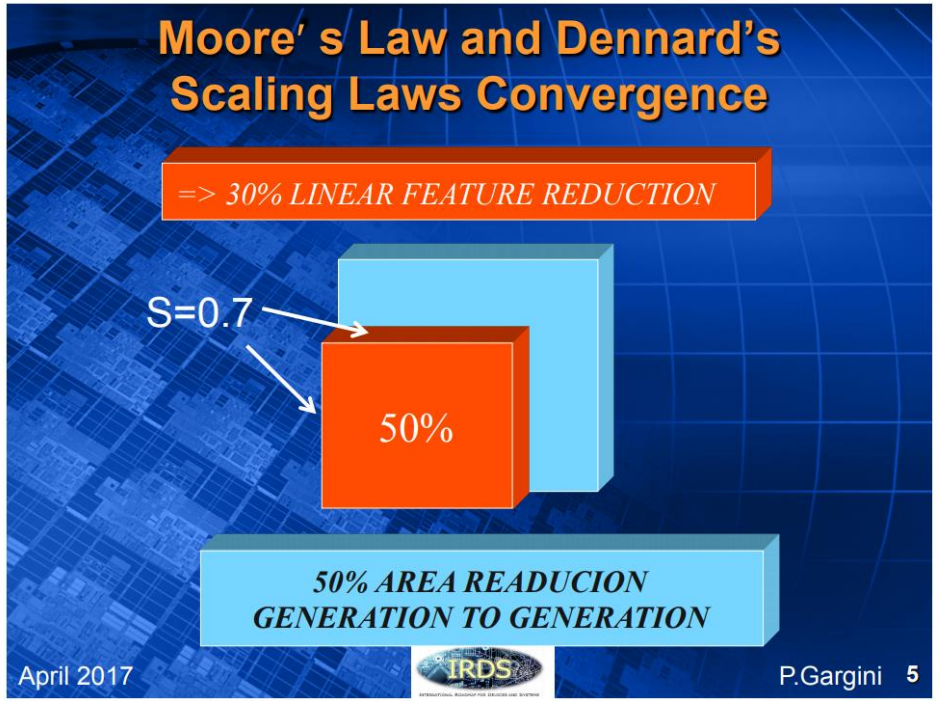
"반도체의 성능이 약 2년마다 2배씩 좋아진다"

Moore's law「2X배/2년」=「50% Area Reduction」

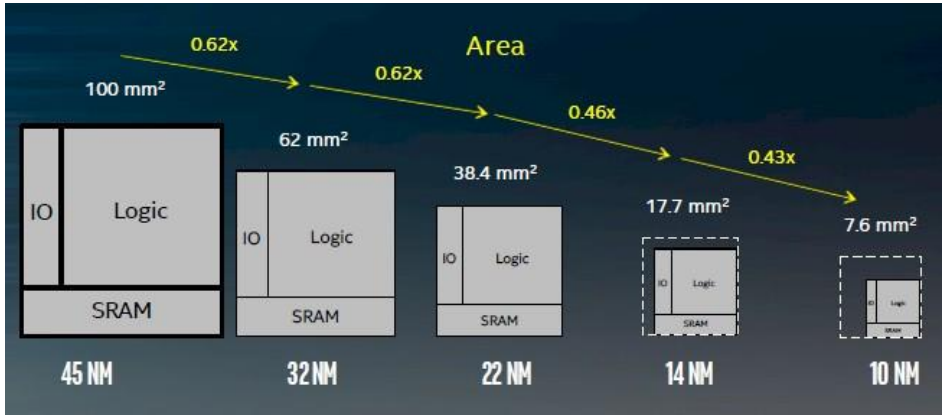
= 30% 선폭 감소 (=X0.7 rule) : 면적 0.7 x 0.7 = 0.49

Node : 32nm → 22nm → 14nm → 10nm → 7nm → **5nm → 3nm**



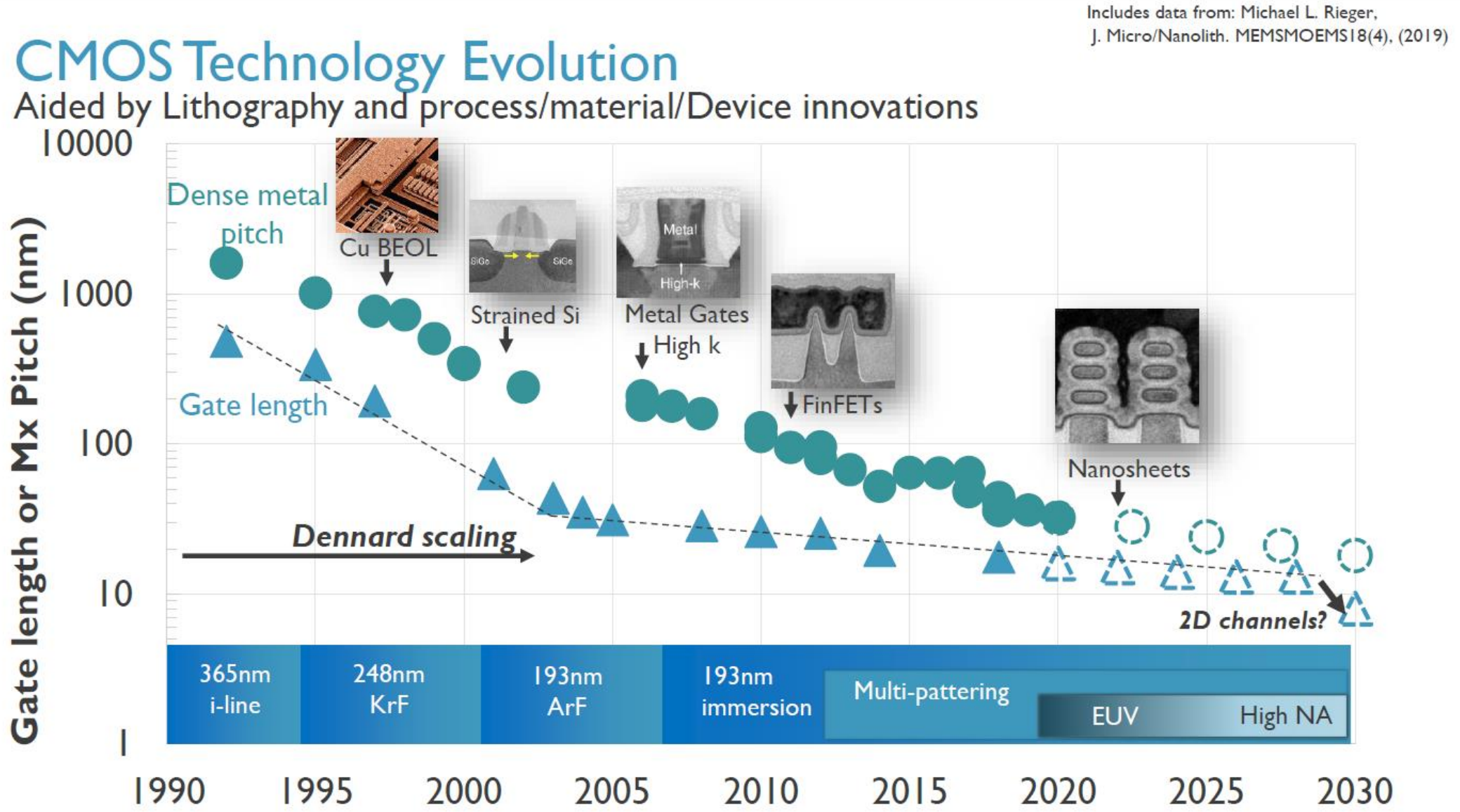


Paolo Gargini (Fellow of IEEE) IRDS 2017



Introduction : More Moore (MM)

Beyond CMOS (Complementary Metal-Oxide-Semiconductor, 상호보완적 금속 산화물 반도체)



Introduction : More than Moore (MtM)

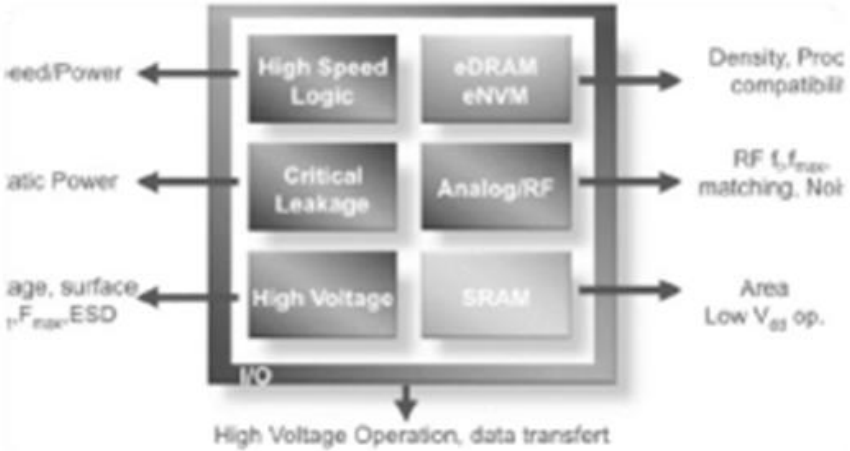
Advanced Packaging (2.5D, 3D)

- higher I/O density
- lower power consumption per bit of data transfer

More than Moore

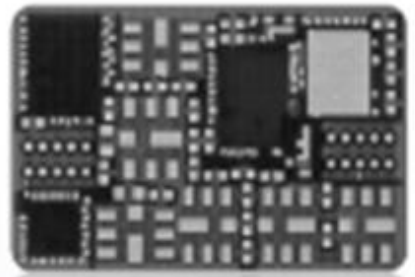
2D SOC (System on Chip)

"All-in-One chip system integration"



Chip area ↑, Cost ↑, Time to Market ↑

3D Packaging

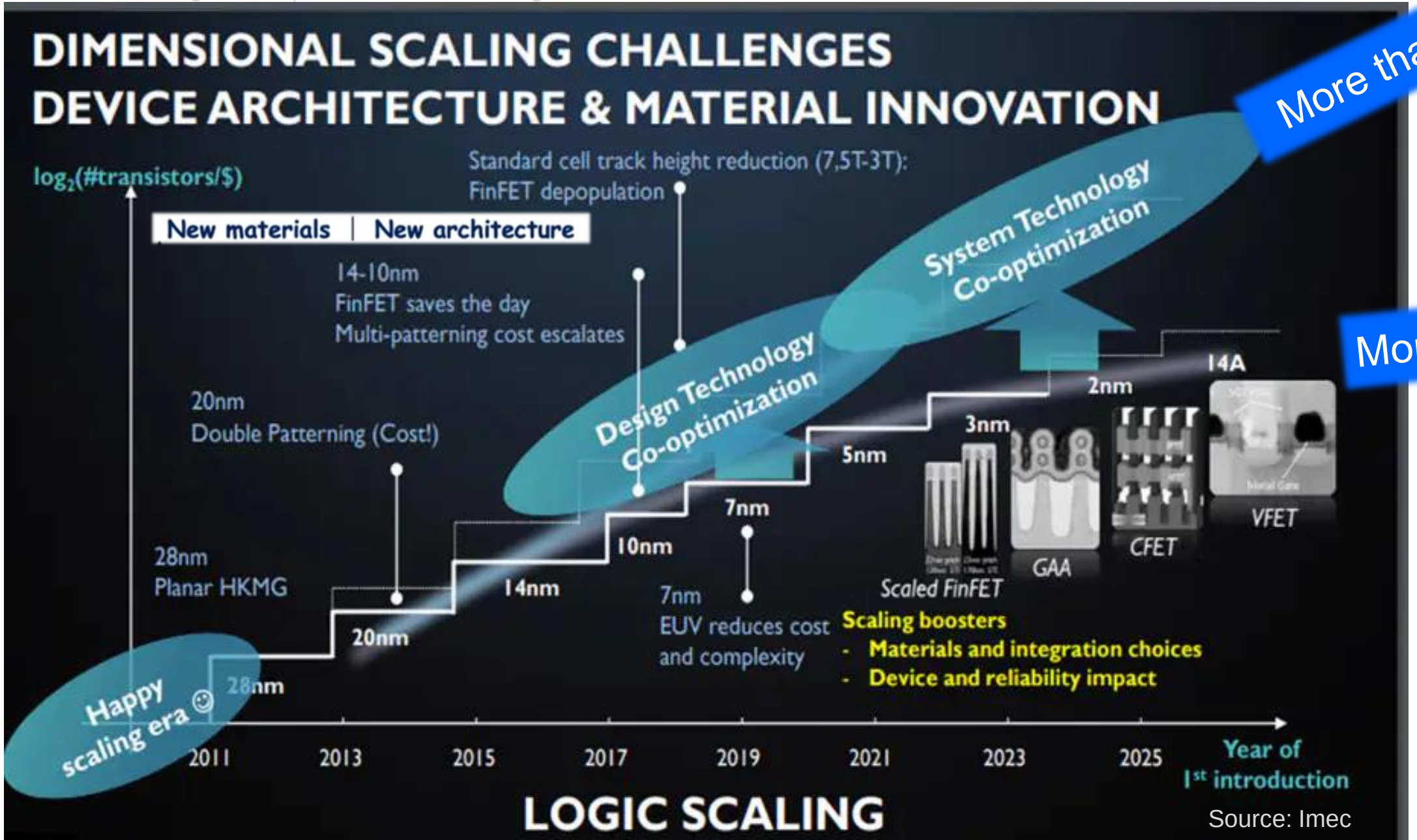


Time to Market ↓, Cost ↓, Performance ↑

Size ↓, Flexibility ↑

Introduction : More Moore & More than Moore (MtM)

Imec's scaling roadmap for semiconductor logic devices



Source: Imec

ULVAC

반도체 기술동향

Introduction of More Moore

- DRAM

- NAND

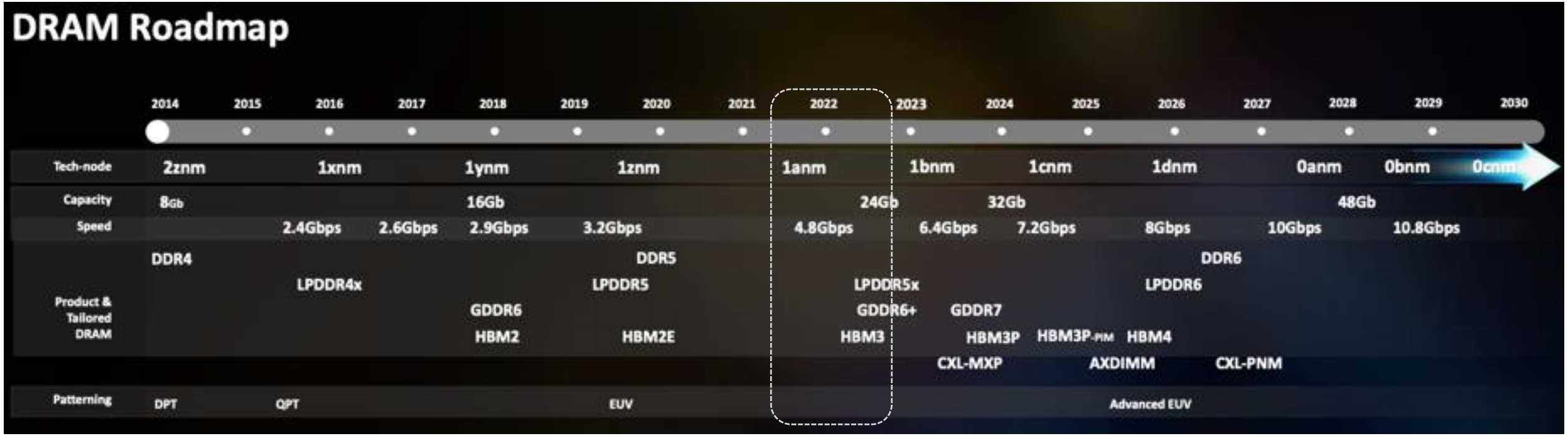
- Logic

power, performance, area, cost, and speed to market,
new design and production paradigms

Introduction of DRAM

Current & Future

Samsung's DRAM Roadmap(SAMSUNG'S MEMORY TECH DAY 2022)



- DDR (i.e. DDR SDRAM, Double Data Rate Synchronous DRAM): for PC or server
- LPDDR(Low Power DDR): for mobile
- GDDR (Graphics DDR),HBM(High Bandwidth Memory) : for GPUs

Samsung 1b DRAM mass production in 2023.
Challenges:
patterning, materials and architecture, High-K material

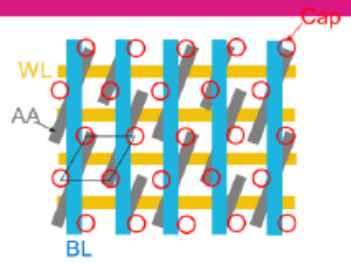
DRAM : 32Gb DDR5 DRAM, 8.5Gbps LPDDR5X DRAM and 36Gbps GDDR7 DRAM.
HBM-PIM(Processing-in-Memory), AXDIMM(Acceleration Dual in-line Memory Module) and CXL(Compute Express Link).

Introduction of DRAM

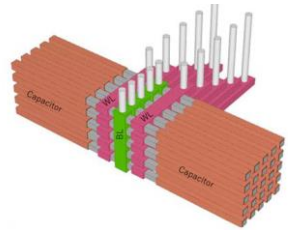
Roadmap

Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027~28	2029~30
F* [nm]	16	15~14		13~12		12~11	≦10	<10	

Cell / Peri. layout: $6F^2$ → 3D



*Feature size: STI hp along WL = STI hp / COS(21°)

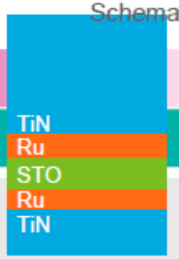


Patterning: 193i SAQP, DP (+ EUV)

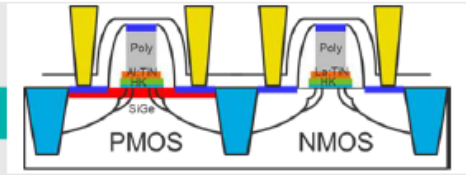
Pillar cap. A.R.: >40 | >45 | >50 | >55 | >60

Capacitor: ZAZ CIP → Alternative: STO etc.

M. Popovici (imec) et al. IEDM 2018
Schematic by TEL



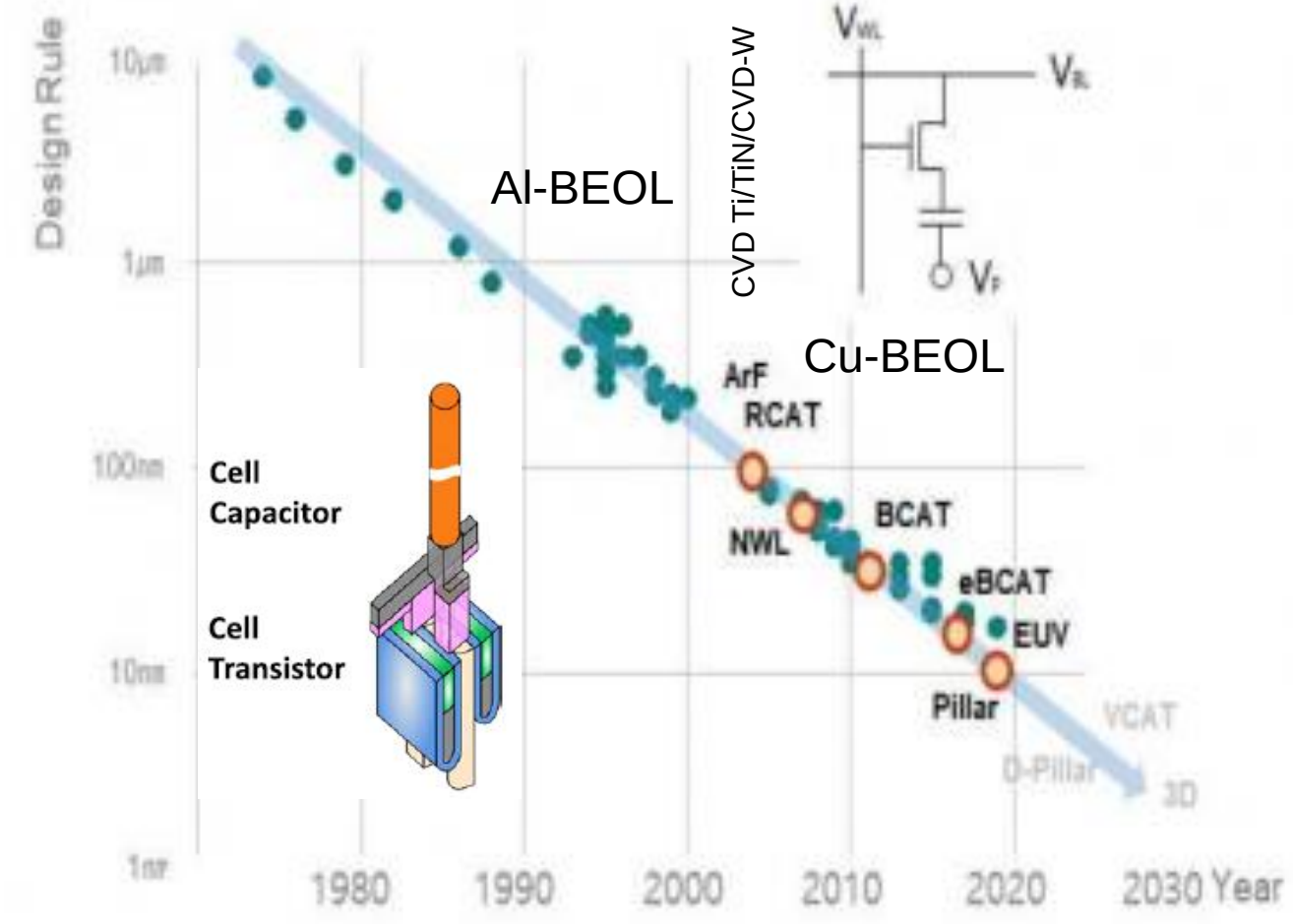
Peri. CMOS: Poly SiON → High-k Metal Gate → FinFET

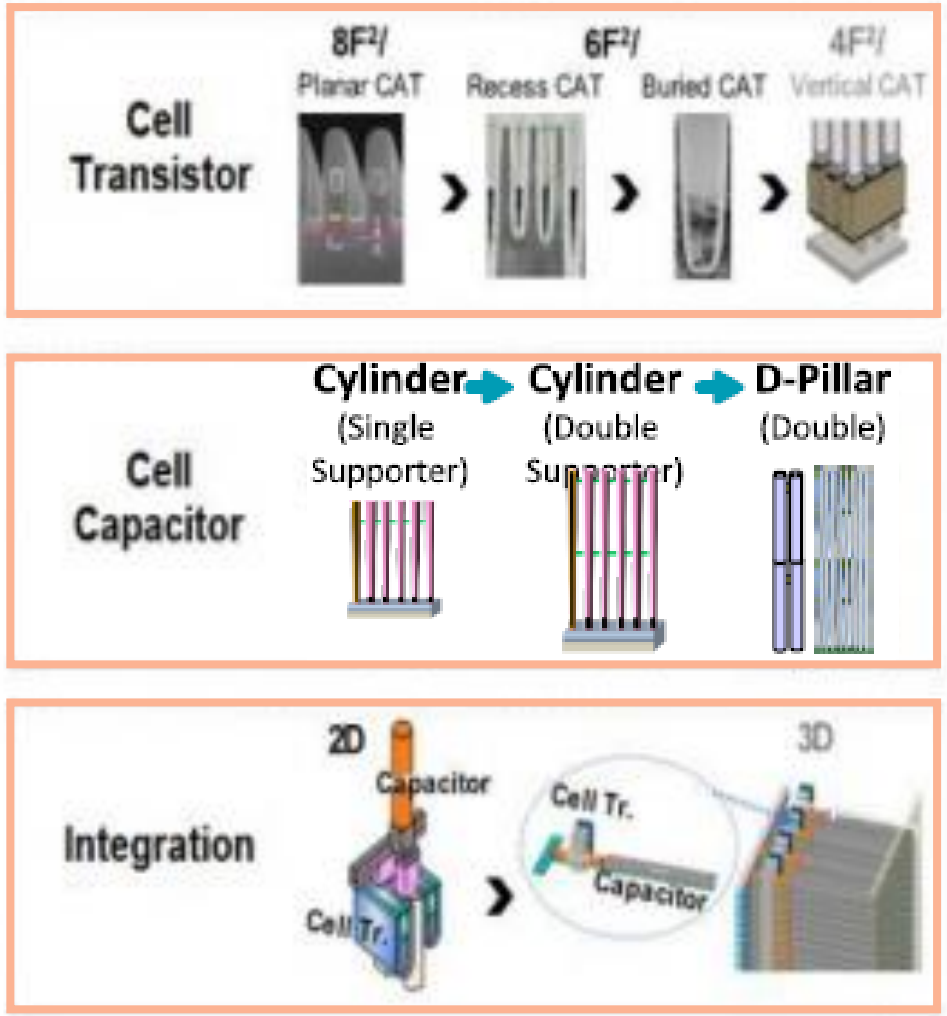


Source: TEL ULVAC

Introduction of DRAM

History (@IEDM2021 Roadmap)





Source: Samsung

Introduction of DRAM

Current & Future

배선(Interconnection) : low-k Oxide, Cu-BEOL, Advanced CuBS
Peri Transistor : High-k Metal Gate

CuBS : Cu Barrier Seed

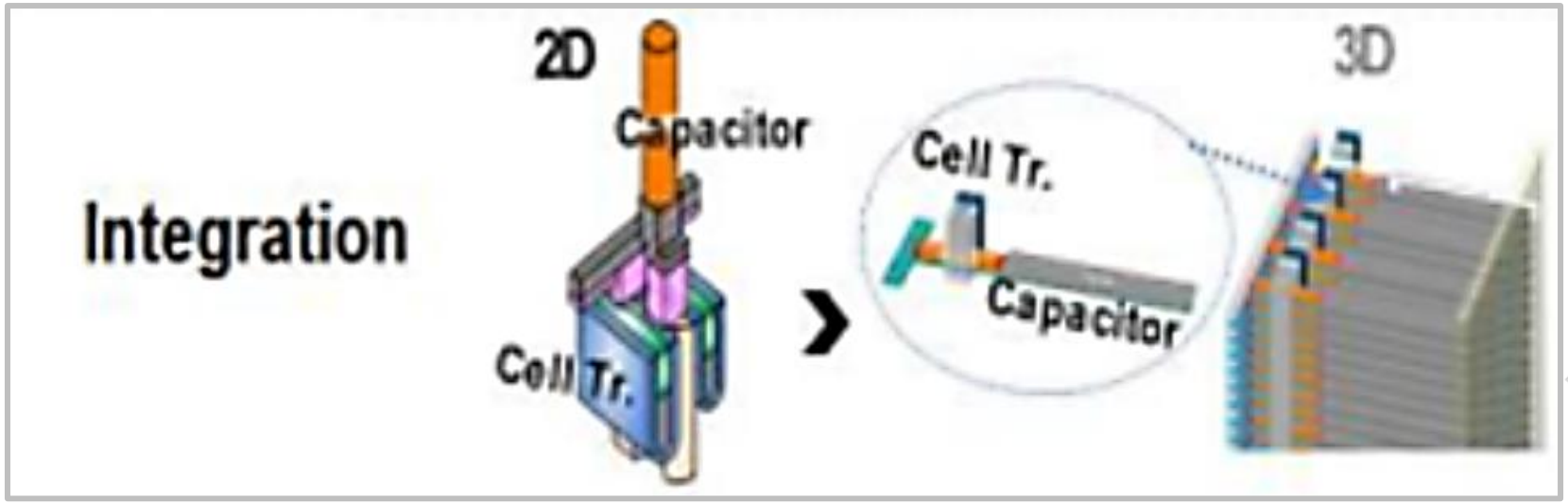
Source: applied materials

Introduction of DRAM

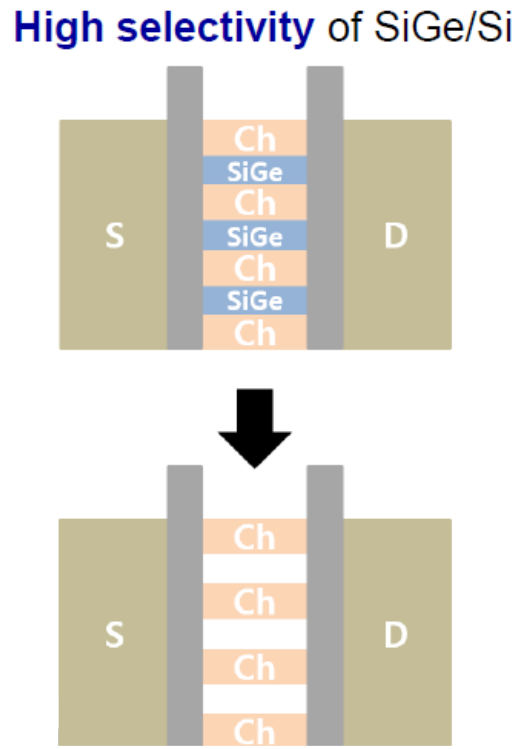
자료: SMC Korea2022

Current & Future

'3D Vertical-DRAM'



IEDM2021 Keynote (Samsung)



Technology:

- New materials
- 3D structure, New Architecture
- HAR (High Aspect Ratio) etch
- ALD, ASD,
- Selective Etch

ULVAC

Introduction of NAND

자료: Semicon Korea2022

Current & Future

Planar → 3D Vertical NAND

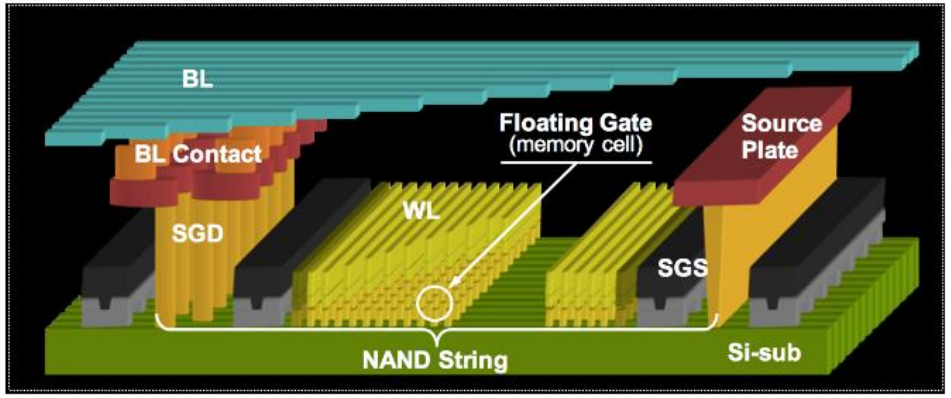


Fig. 1: 2D NAND architecture. Source: Western Digital.

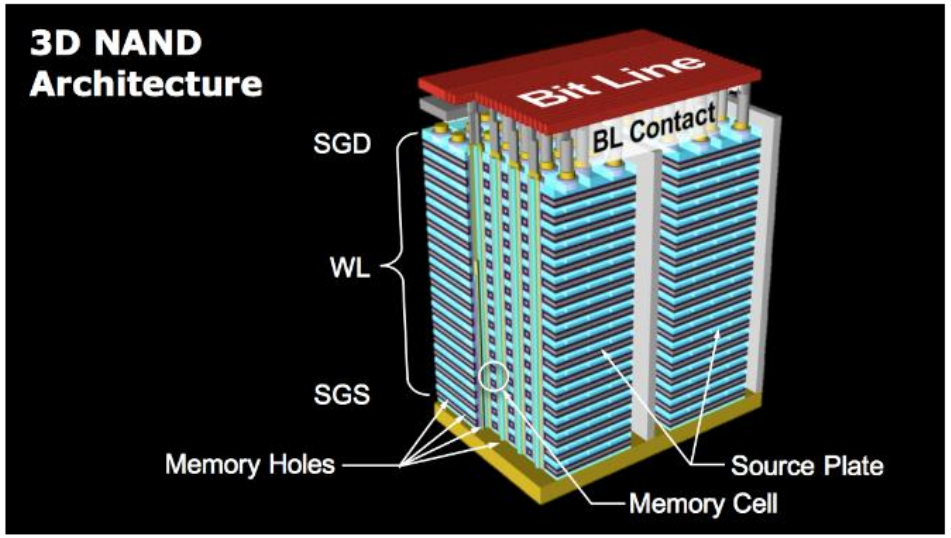
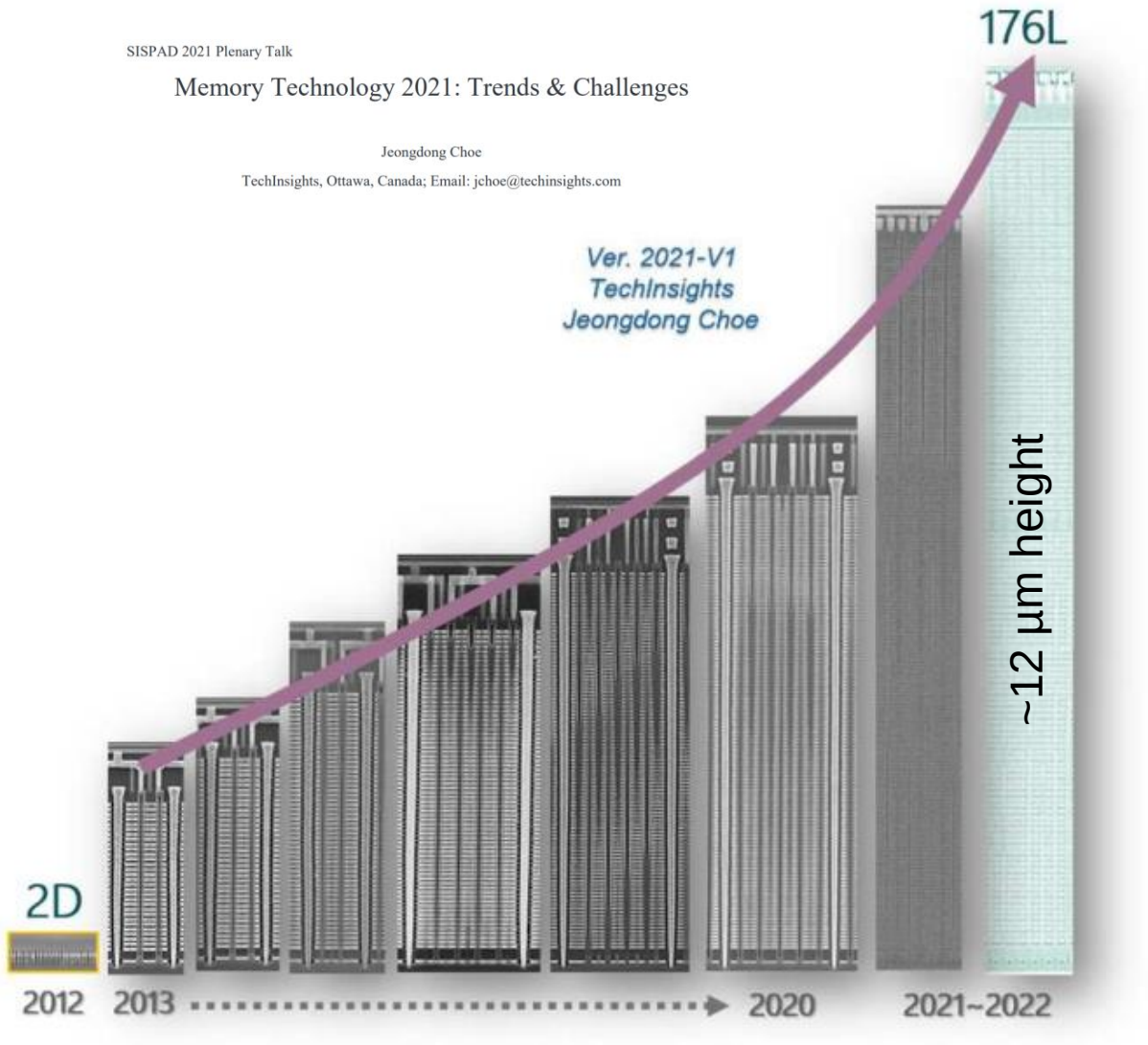


Fig. 2: 3D NAND architecture. Source: Western Digital



Introduction of NAND

Current & Future

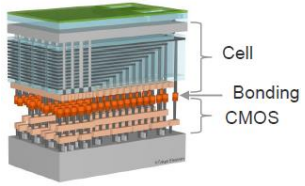
Samsung's VNAND Roadmap(SAMSUNG'S MEMORY TECH DAY 2022)

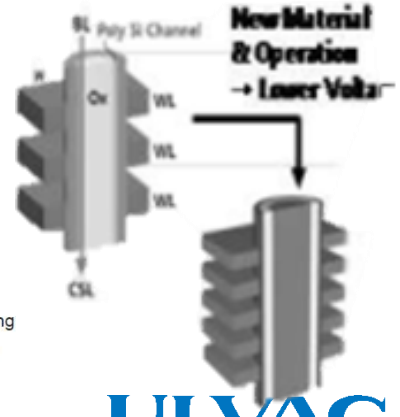
V-NAND V9, mass production in 2024.
1,000+ V-NAND Layers by 2030.

Cell on Peri

Multi stack

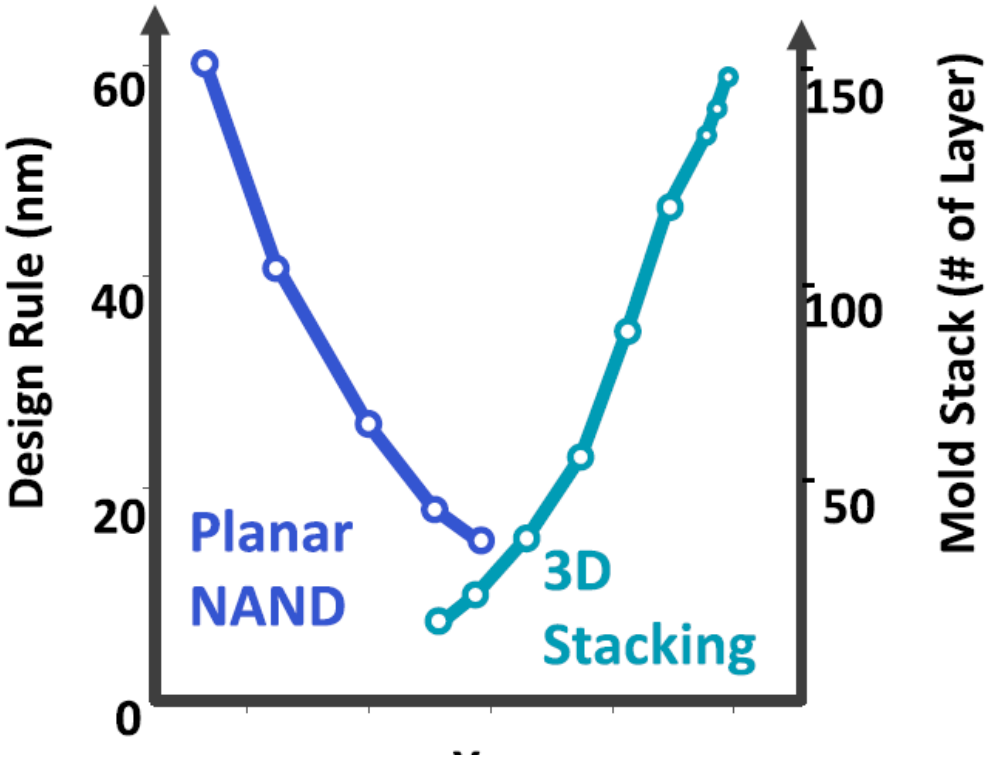
Wafer Bonding

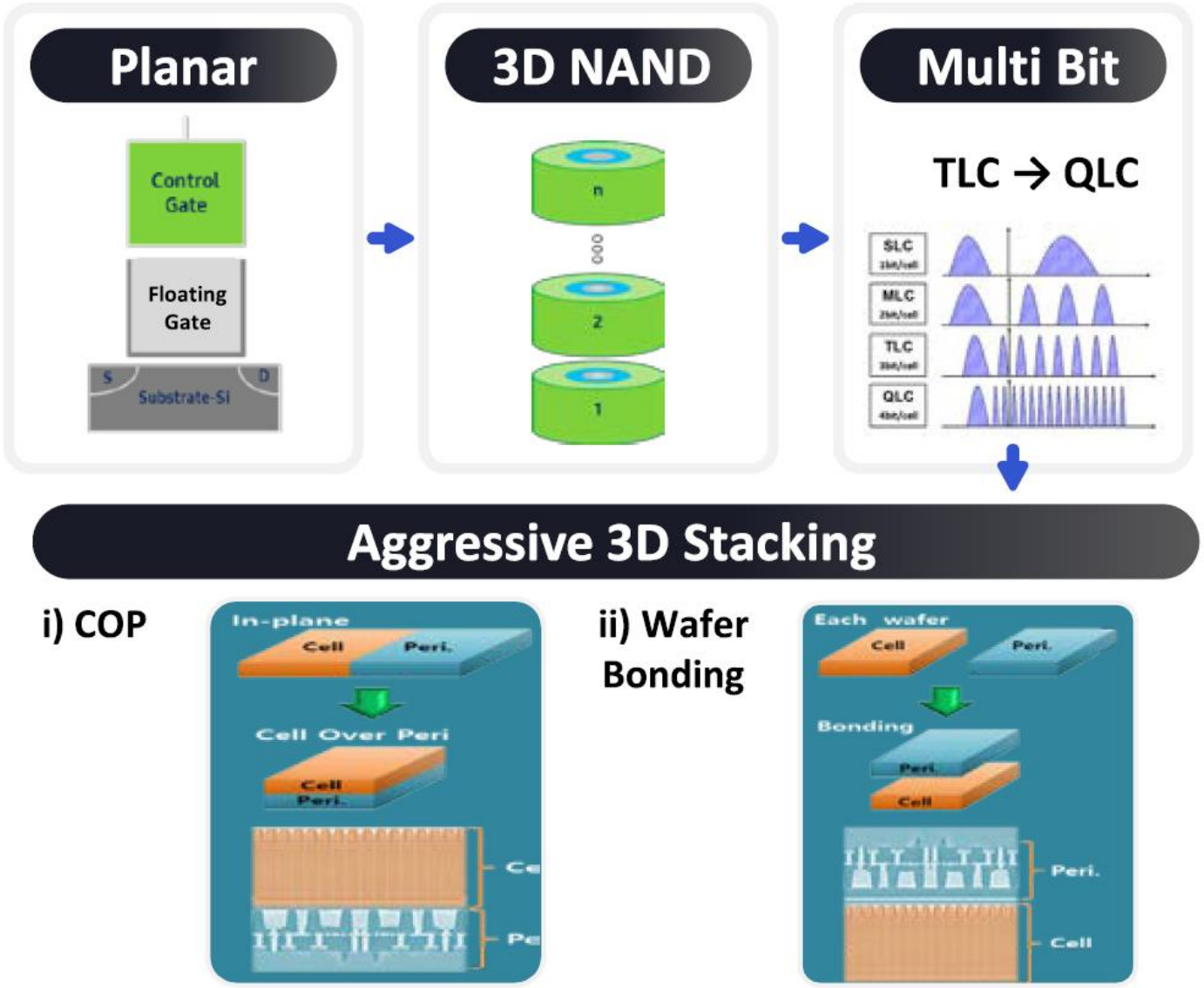




Introduction of NAND

Current & Future



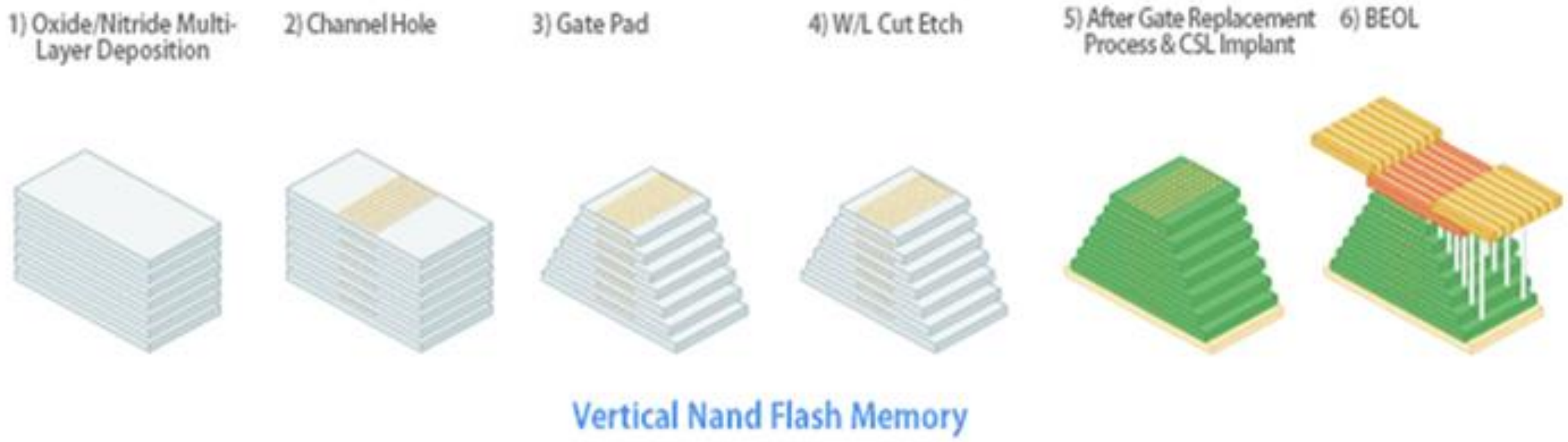


※ COP : Cell Over Peripheral, TLC : Triple Level Cell, QLC : Quadruple Level Cell

Source: Semicon Korea2022, Samsung

Introduction of NAND

Current & Future



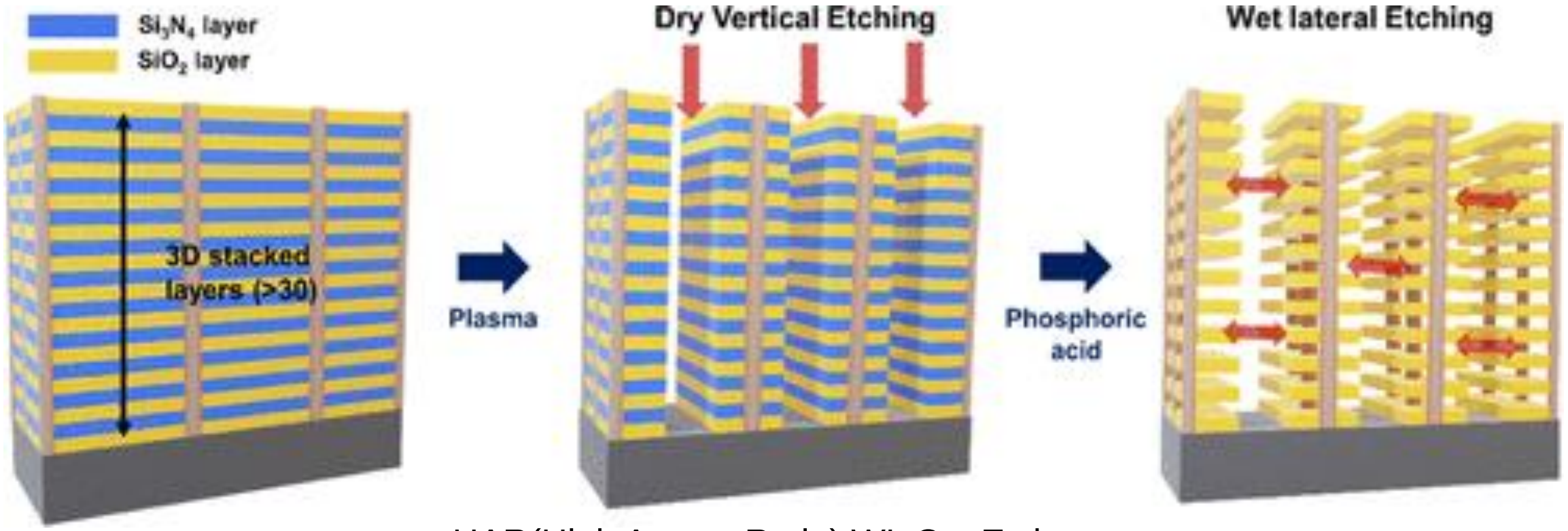
- Ultra Low Thickness uniformity Mold(Oxide/SiN)
- HARC(High Aspect Ratio) Etch
- 고 선택비 wet etch
- Double stack integration
- ALD ONO & Poly Si deposition

- WL & Interconnection W
- Deep MC Contact (COP)
- Cu BEOL

- Stair(Gate Pad) etch & Raised PAD

Introduction of NAND

Current & Future



- HAR(High Aspect Ratio) WL Cut Etch
- 고 선택비 wet etch
- Double stack integration
- Low resistivity WL materials (ALD W, ALD Mo)
- Dry clean
- Warpage (wafer stress)


Green Manufacturing of Silyl-Phosphate for Use in 3D NAND Flash Memory Fabrication

Hyun Il Lee, Hyun Su Kim, Elsa Tsegay Tikue, Su Kyung Kang, Haoxiang Zhang, Ju Won Park, SeungHwa Yang, and Pyung Soo Lee*

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자료: ACS(American Chemical Society)

Introduction of NAND

Current & Future

Film deposition
- stress control

Bevel etch
Backside Depo

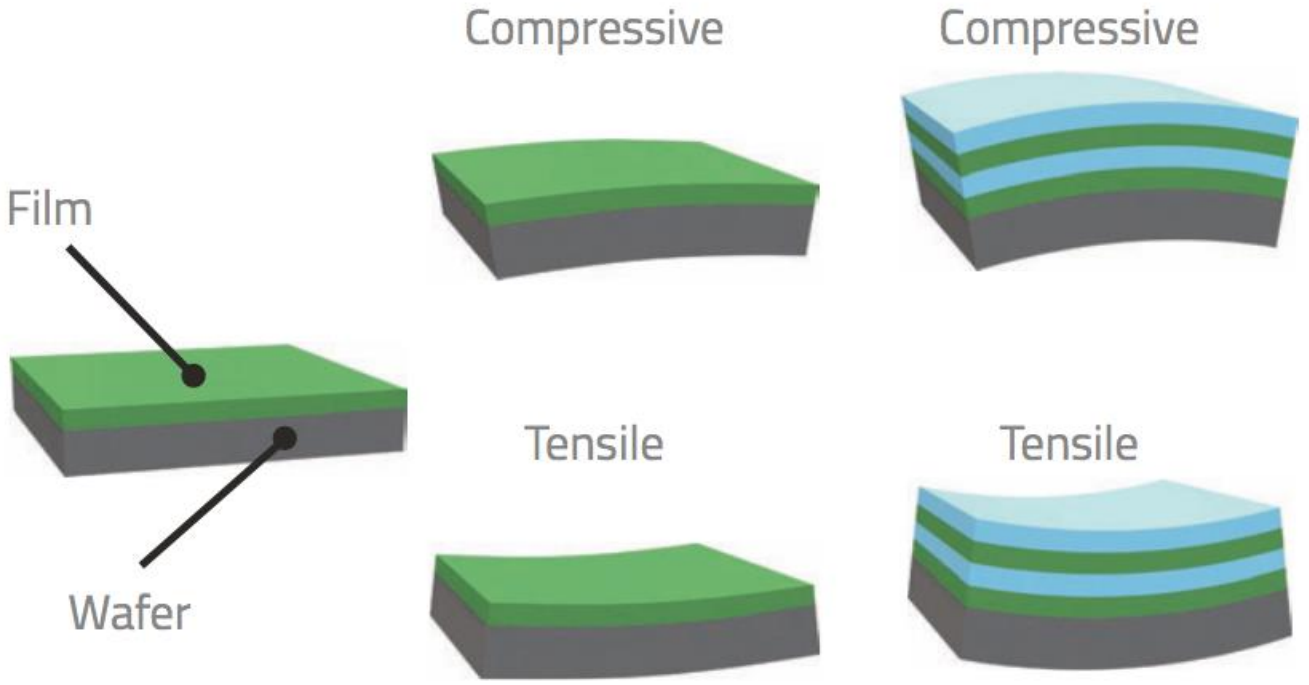


FIGURE 2. As the number of layers increases in the 3D NAND device, the effect of film stress can become magnified.

Introduction of NAND

Current & Future

Staircase etch

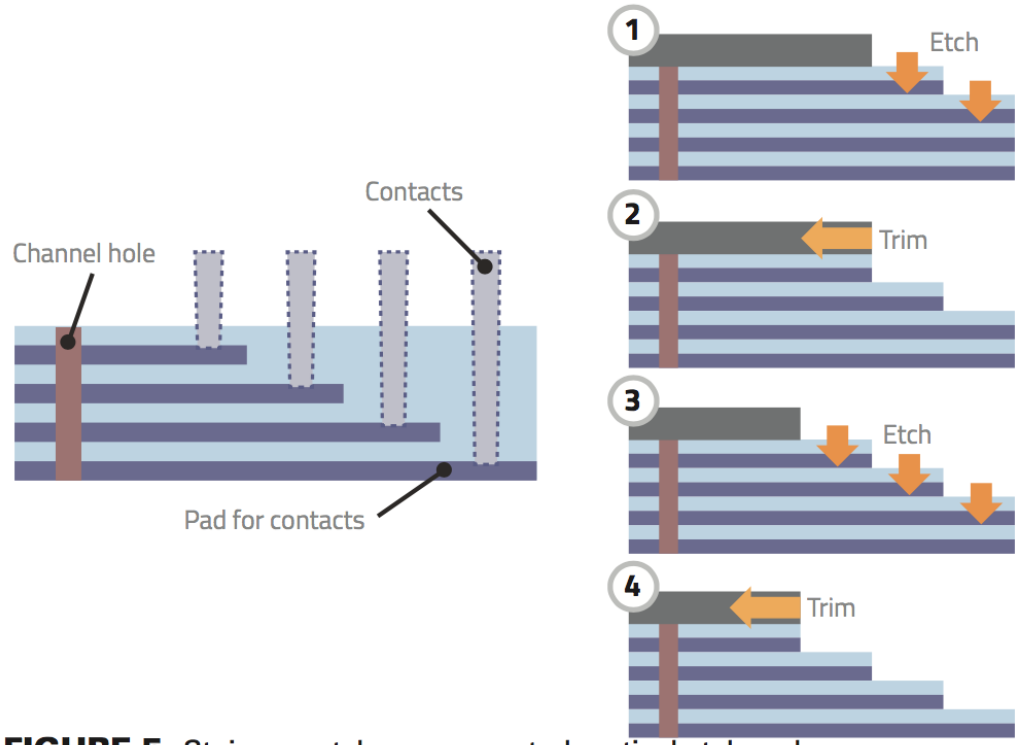
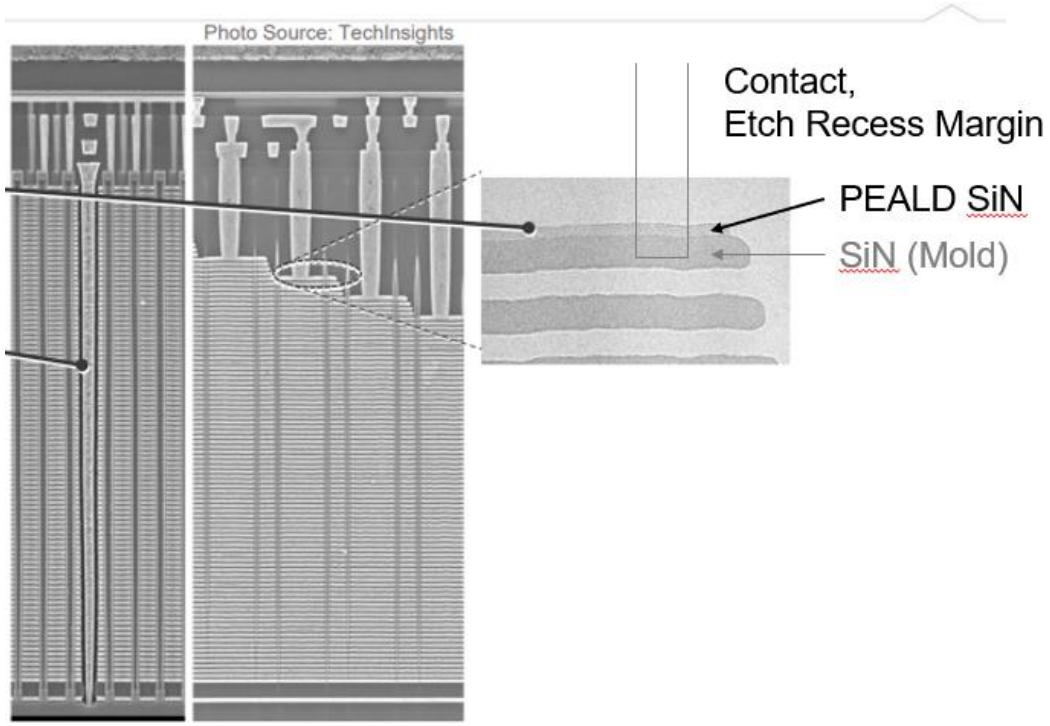


FIGURE 5. Staircase etch uses repeated vertical etch and lateral trim etch passes to define the contact pads.

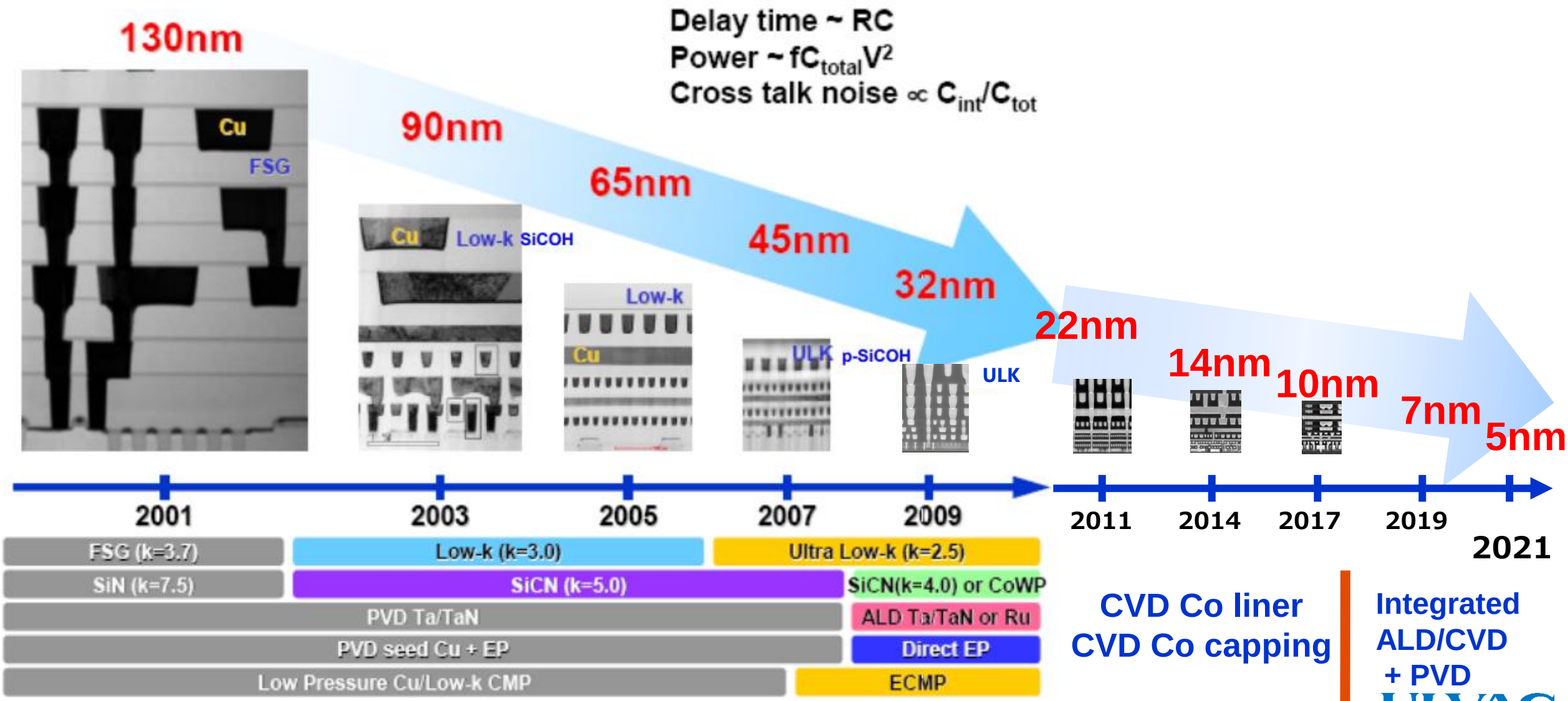
Staircase(WL MC PAD) PEALD application



Source: ASMI Analyst and Investor Technology Seminar July 9. 2019

Introduction of Logic

Logic Node Scaling & Metal



CVD Co liner
CVD Co capping

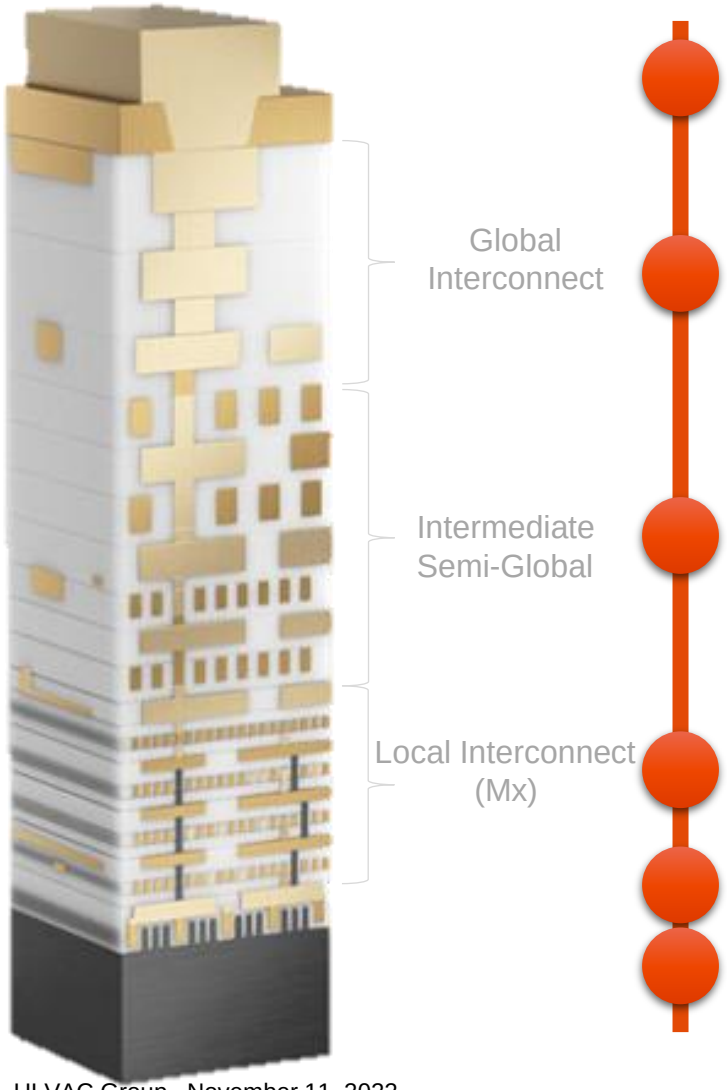
Integrated ALD/CVD + PVD

ULVAC

H.-K. Kang, tutorial on Advanced Logic Technology, 2007

Introduction of Logic

Logic 10nm



Al PAD

Cu BEOL (Back End of Line)
Global Interconnect

Cu BEOL – small pitch

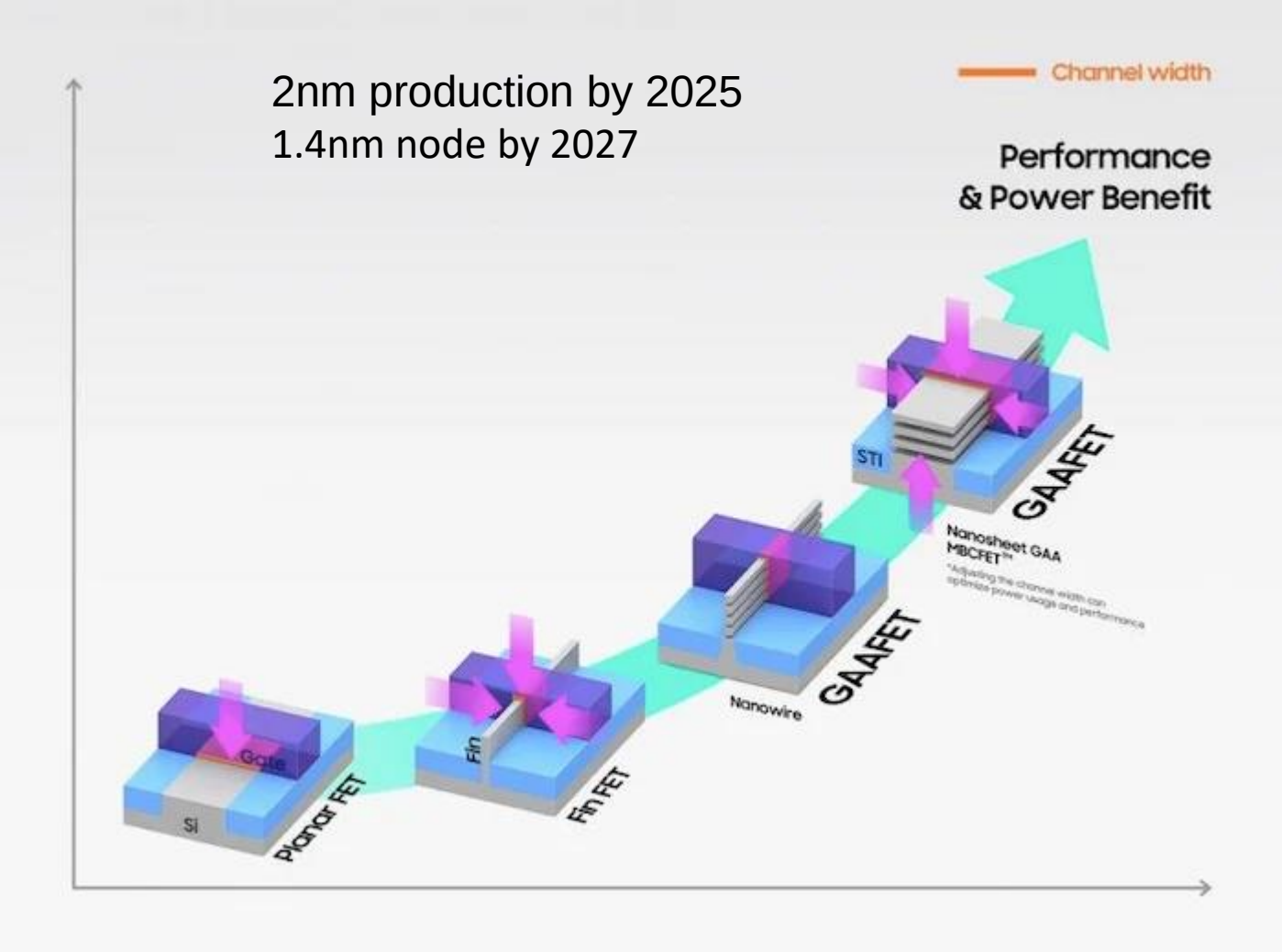
MHM-TiN: Metal / Via - Dual damascene pattern

Cu BEOL –「Minimum Metal Pitch (MMP)」

MOL (Middle of Line)
FEOL (Front End of Line) – FinFET, GAA, HKMGs

Introduction of Logic

FEOL – Transistor

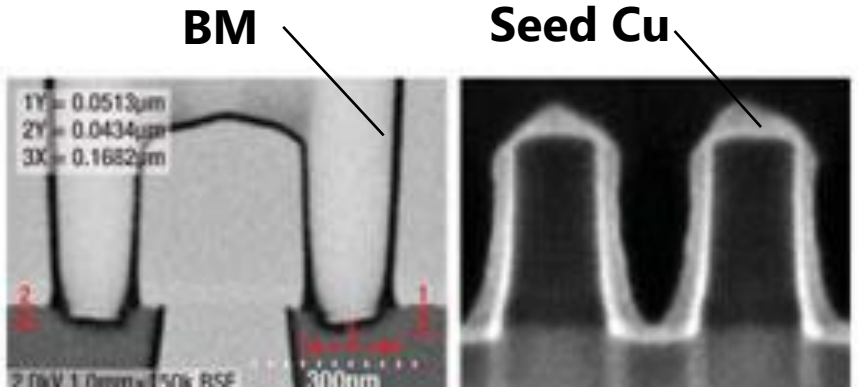


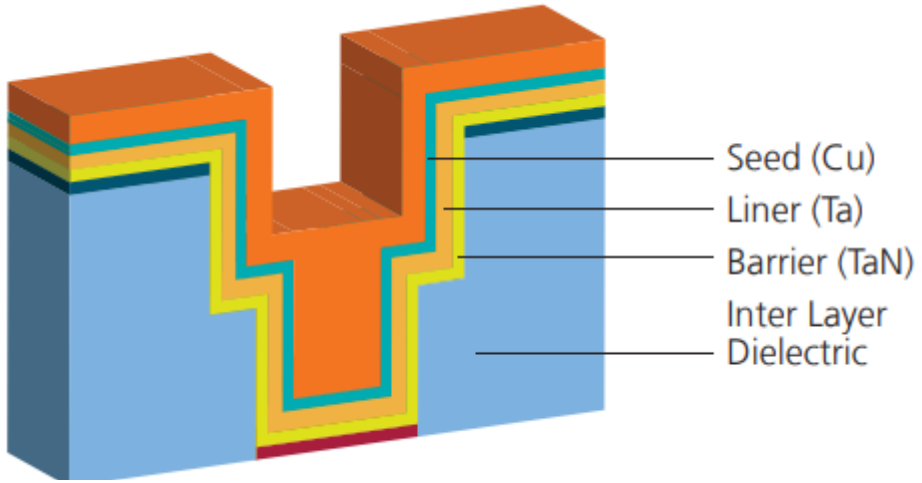
Introduction of Logic

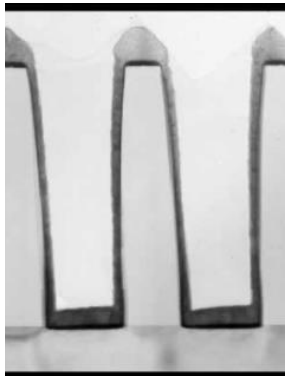
BEOL – Metallization Process

Low Resistance interconnect

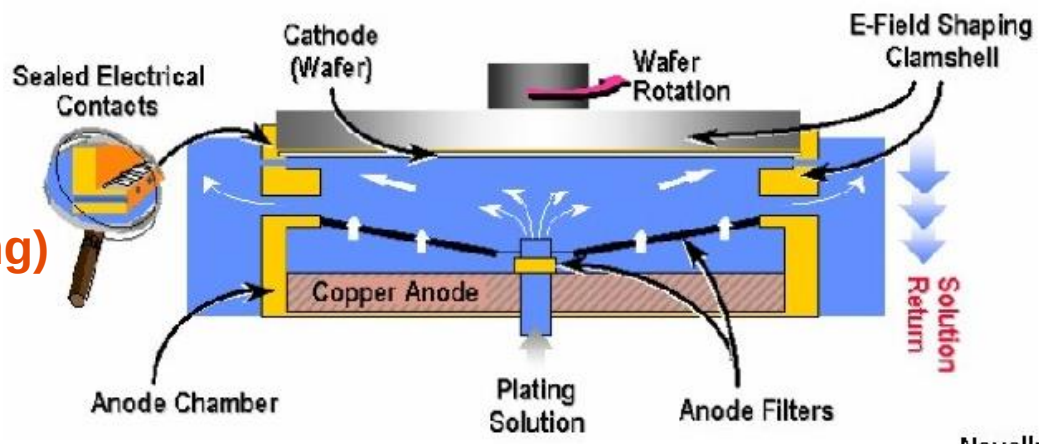
BM
Seed Cu

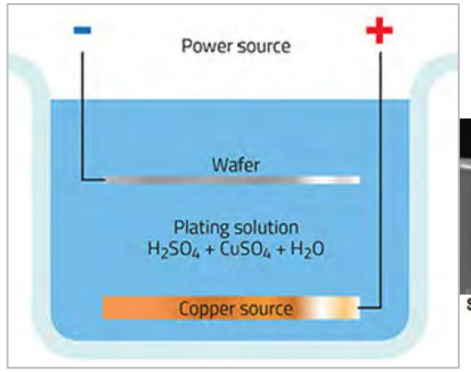






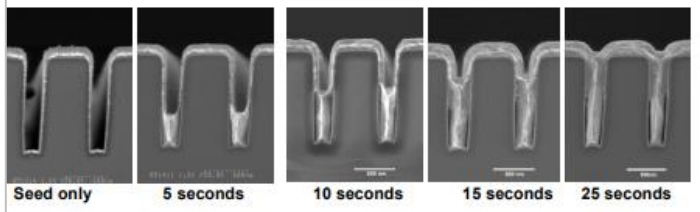
EP Cu
(Electro Plating)





Novellus

EP Cu (Bottom-up)



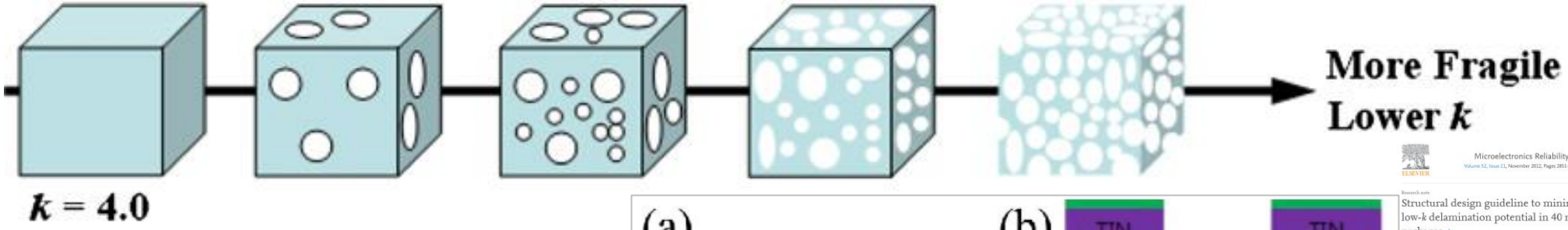
$Cu^0(solid) = Cu^{+2}(aq) + 2e^-$

Introduction of Logic

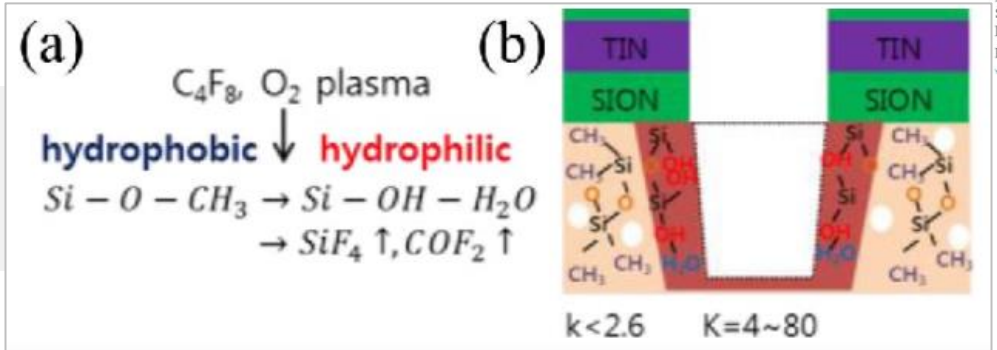
-Low-k (Dielectric constant k-value) → ULK(Ultra Low-k)

pSiOCH

- Porosity lowered the film's dielectric constant, k,
- reduce the interconnect wiring capacitance contribution to the **RC signal delay** in integrated circuits. (*Resistance & Capacitance Delay)
- PID (Plasma induced Damage) → change k-value up



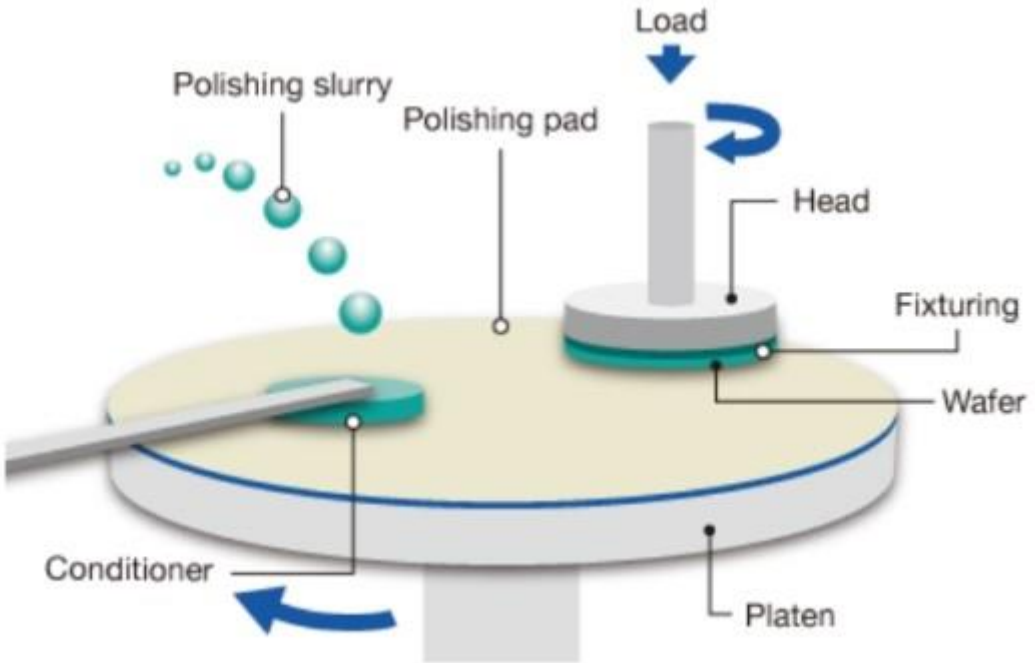
Plasma Damage:
(a) Chemical formula of low-k material after PID and etch byproducts
(b) (b) Structure of porous-SiCOH pattern after PID
(*PID: Plasma Induced Damage)



Introduction of Logic

-Cu CMP (Chemical Mechanical Polishing)

- CMP removes and planarizes Cu on the wafer's front surface
- Rotating pad (mixture of chemicals and abrasives)
- Post-clean : rinse, dry



CMP process schematic diagram

Introduction of Logic

Wafer Backside interconnection, backside bonding: Power rail

PDN : Power Distribution Network

Samsung to use BSPDN (Backside-PDN) tech for 2nm chip

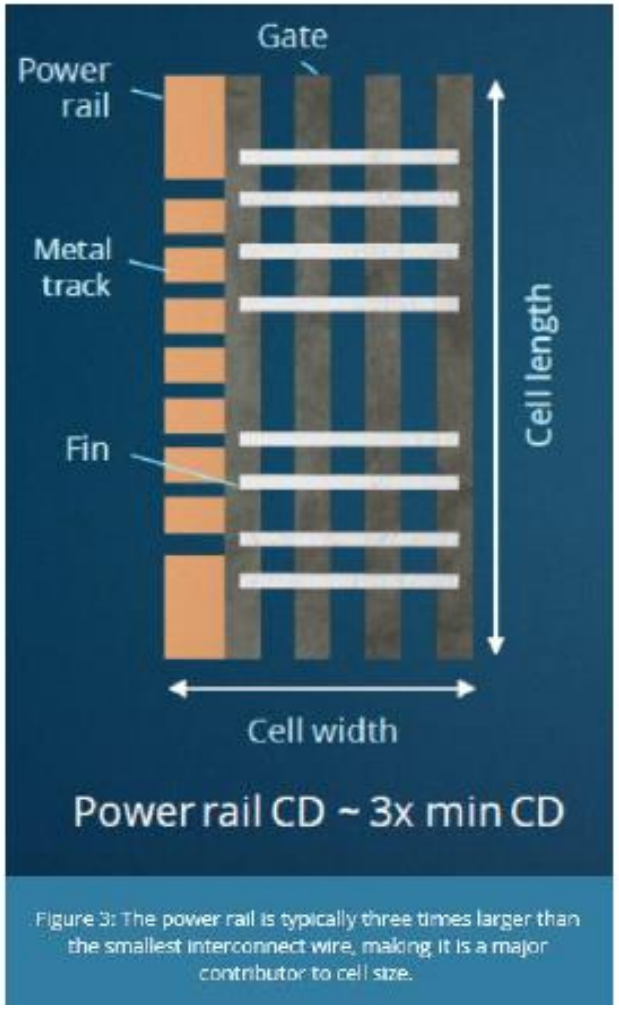


Figure 3: The power rail is typically three times larger than the smallest interconnect wire, making it is a major contributor to cell size.

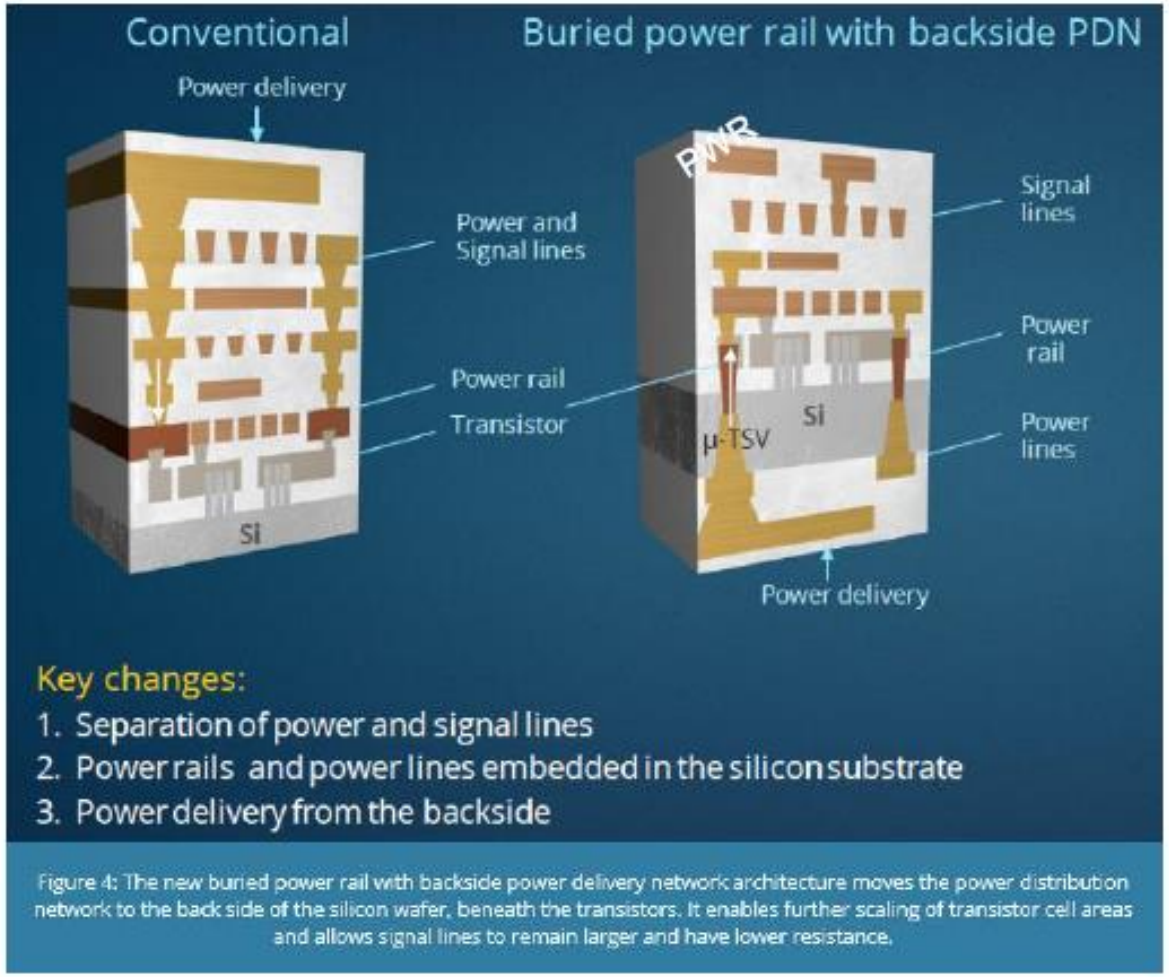
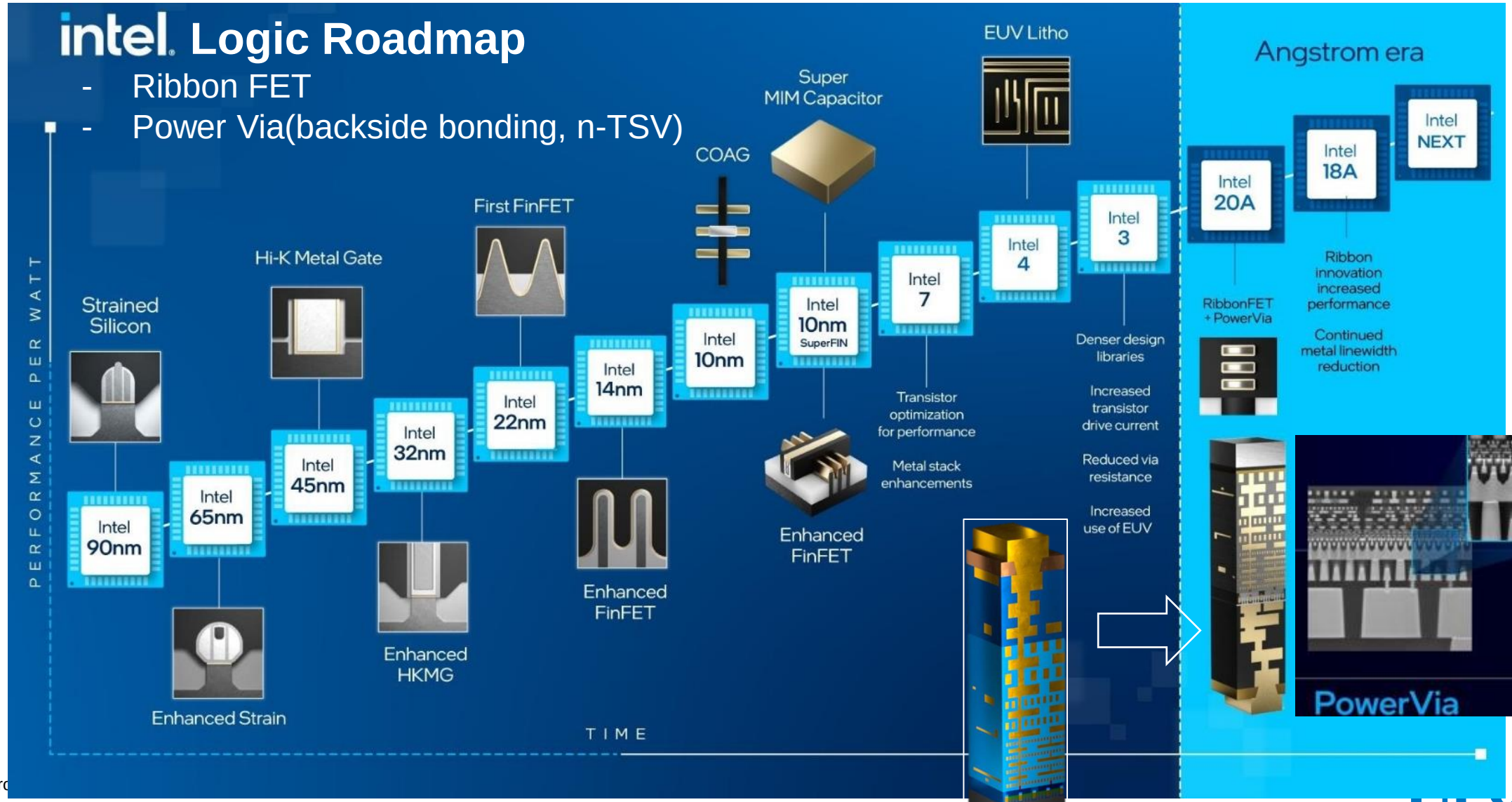


Figure 4: The new buried power rail with backside power delivery network architecture moves the power distribution network to the back side of the silicon wafer, beneath the transistors. It enables further scaling of transistor cell areas and allows signal lines to remain larger and have lower resistance.

Source: applied materials

Introduction of Logic

Intel Logic Roadmap



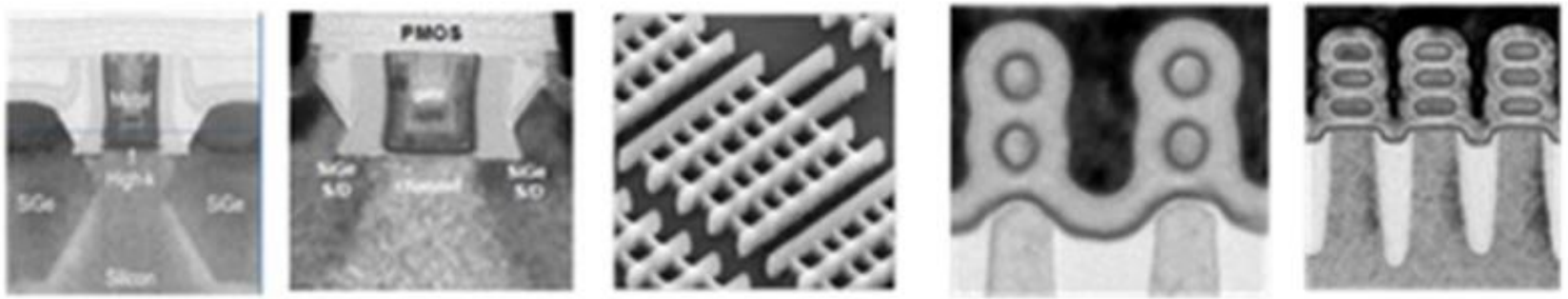
Source: Intel

Introduction of “More than Moore”

Transistor Level

Moore's Law

the number of transistors would double every two years.



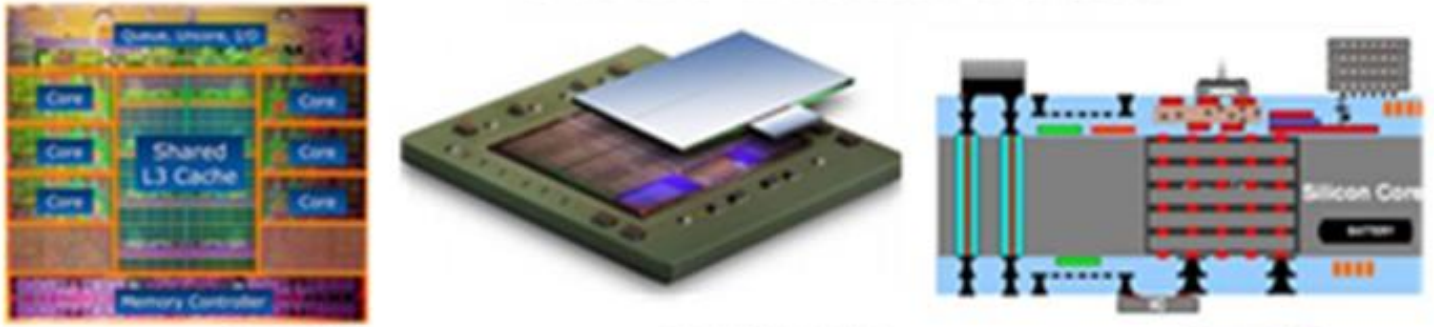
physical limitations to transistor scaling

1947

Planar device → 3D devices

System Level

More Than Moore



2D → 2.5D → 3D

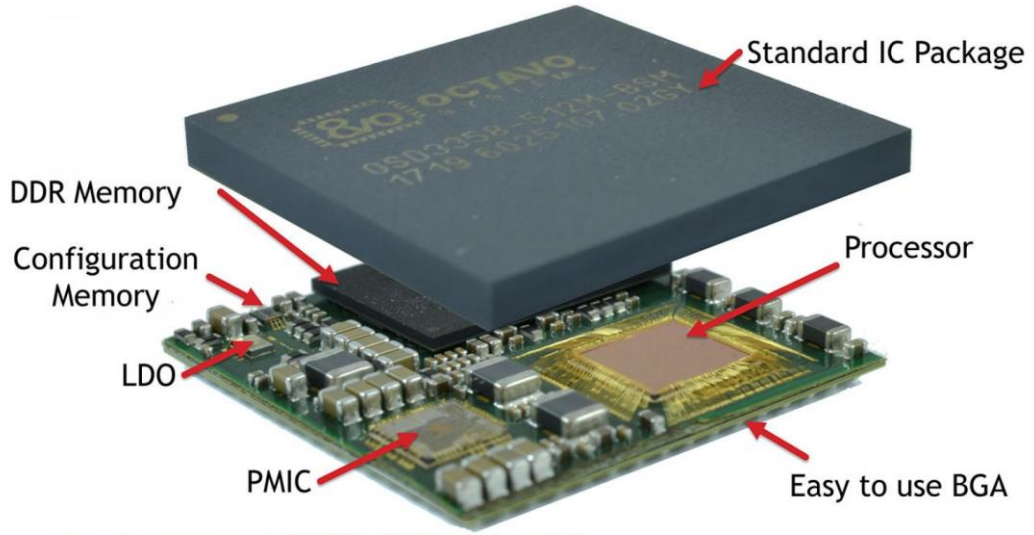
- Quicker time to market
- Lower cost
- Improved performance
- Reduced size and space
- More flexibility

https://trh.gase.most.ntnu.edu.tw

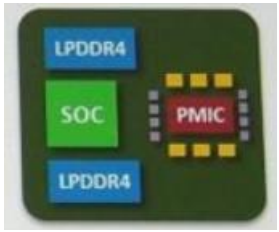
Introduction of Package

SiP (System in package)

하나의 패키지 안에 여러 개의 칩을 적층 또는 배열



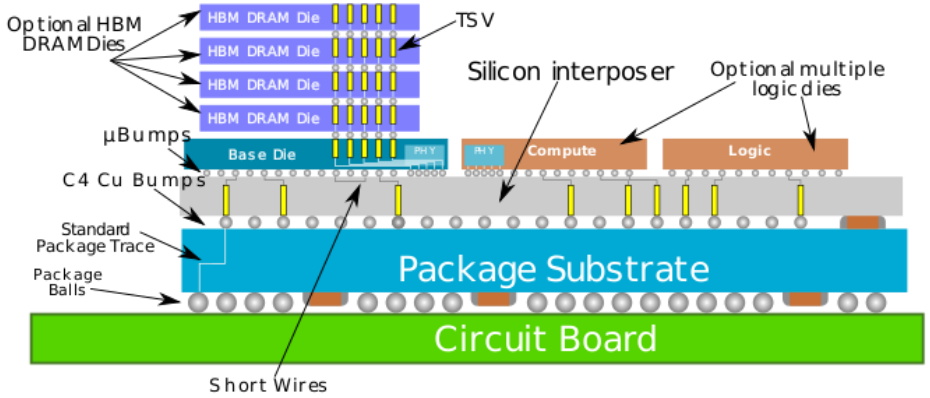
圖五、Apple Watch S1 處理器模組可望採用日月光 SiP 封裝



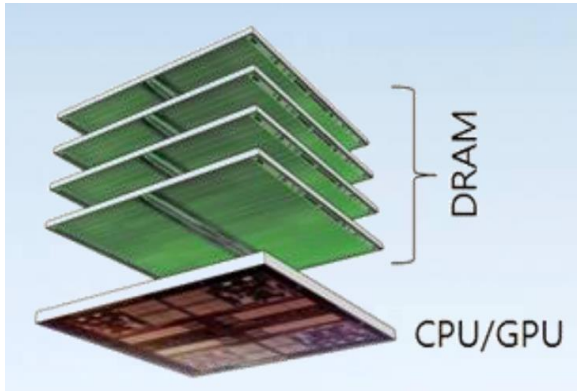
Exynos auto(SoC / SiP)

Advanced Package 2.5D/3D

2.5D (Interposer Stacking)



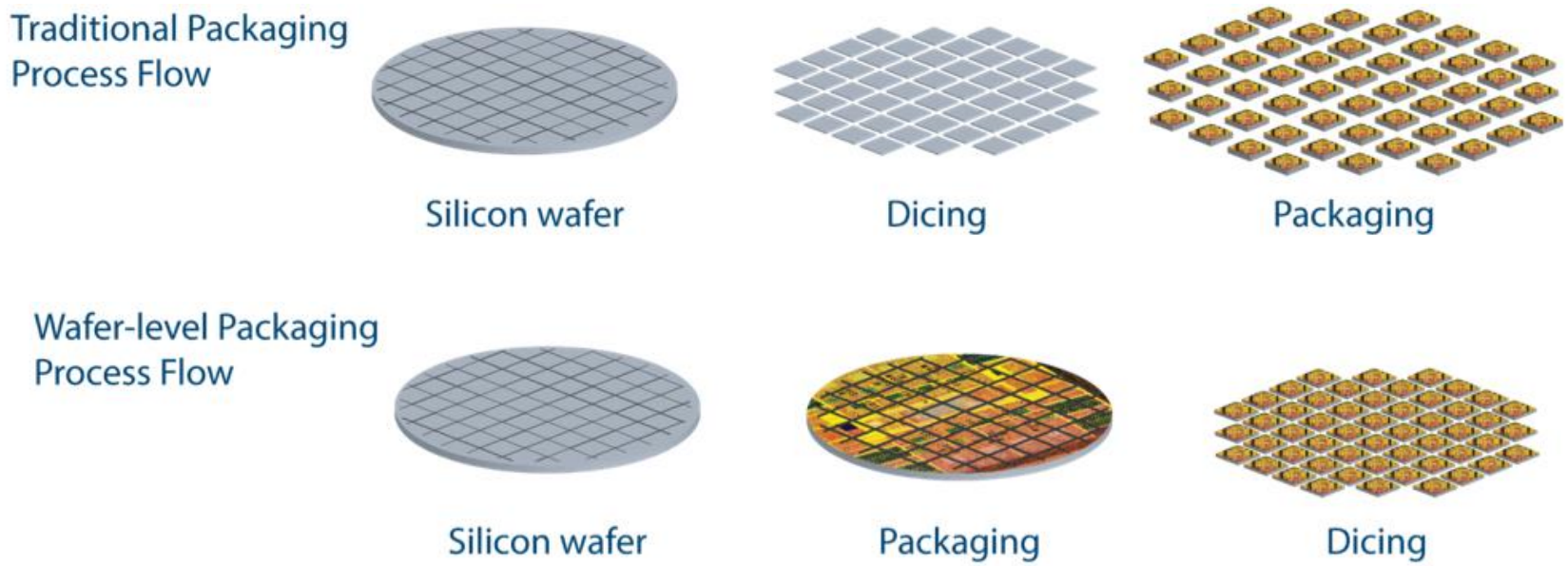
3D (Vertical Stacking)



Introduction of Package

● Wafer Level Package(WLP)

WLP는 Wafer 통째로 Package를 진행하여 낱개의 칩으로 잘라내는 것
WLP는 반도체 공정을 이용 반도체 기판과 같은 RDL(Redistribution Layer)로
반도체 Chip과 외부신호를 연결



Source: www.brewerscience.com

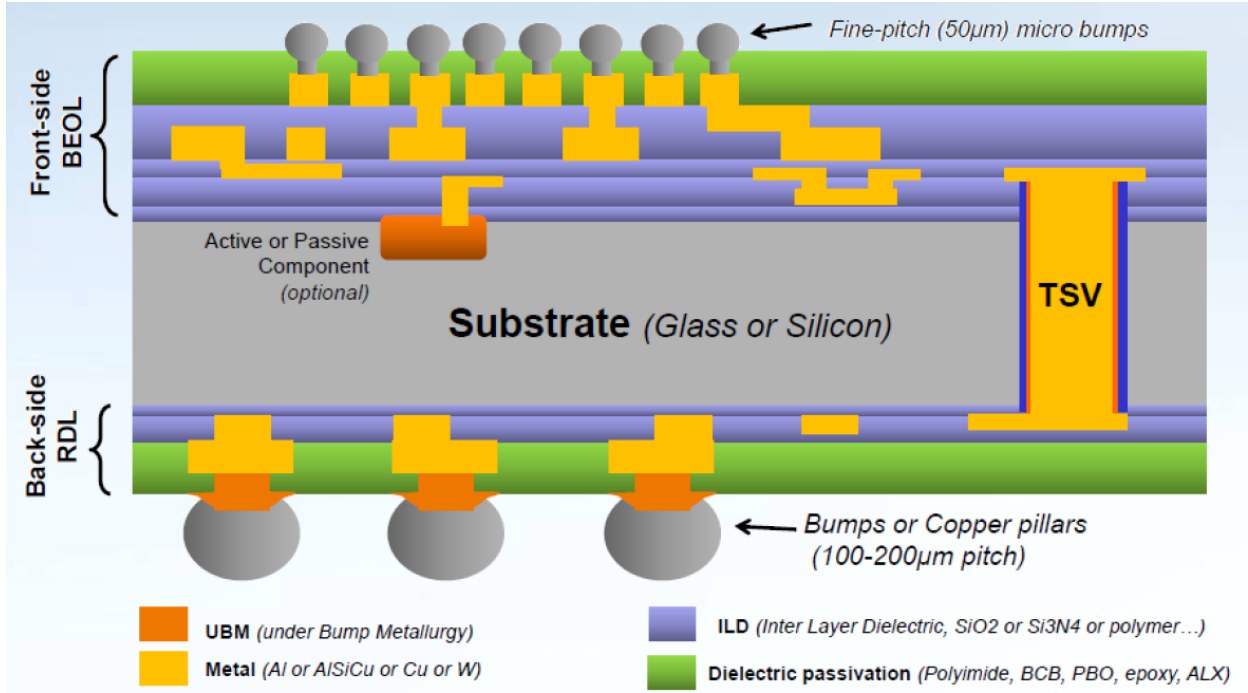
Introduction of Package

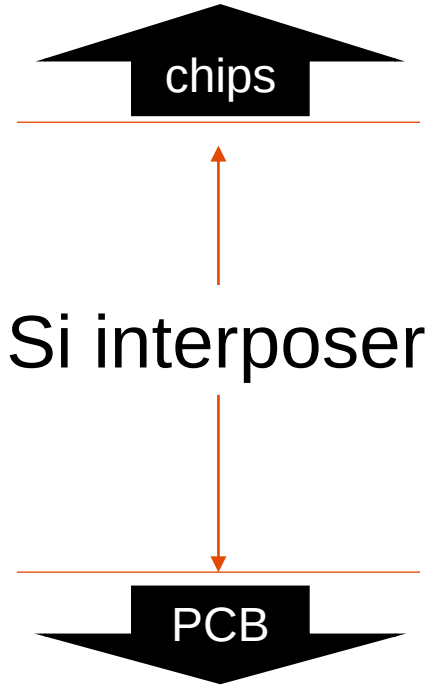
Si Interposer

- Buffer : 3-D interconnection에서 이종 chip 사이에 삽입되어 재배선 및 buffer 역할
- Fine Pitch Si Substrate : 다수의 chip을 integration 하는데 사용되는 silicon substrate

→ 기존 organic substrate에 비해 high wiring density 제공 가능

- 실리콘 인터포저를 통해 집적도를 높인 후 기판과 신호를 주고받는다.



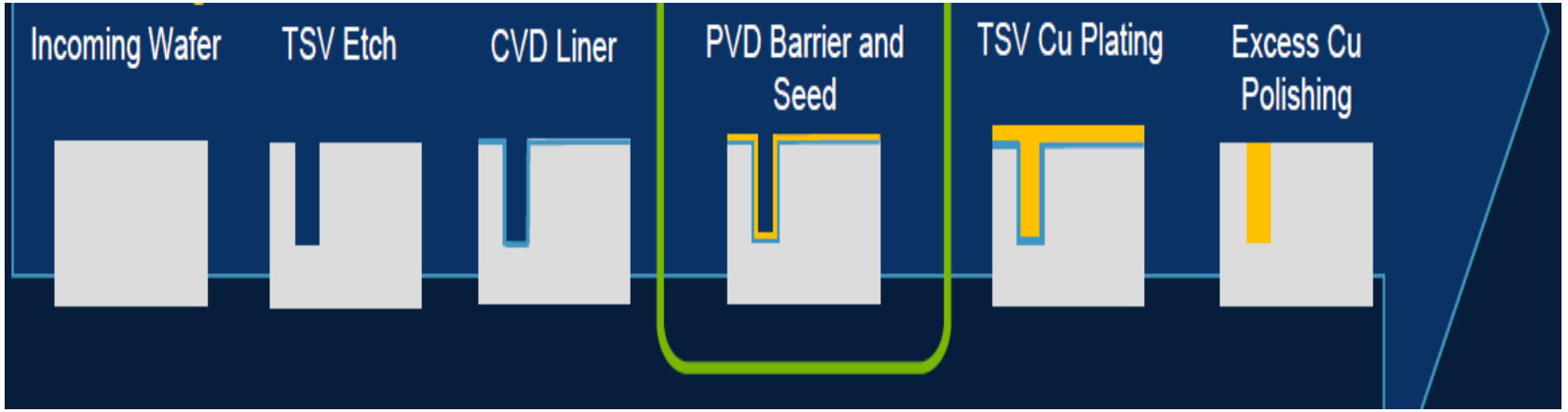


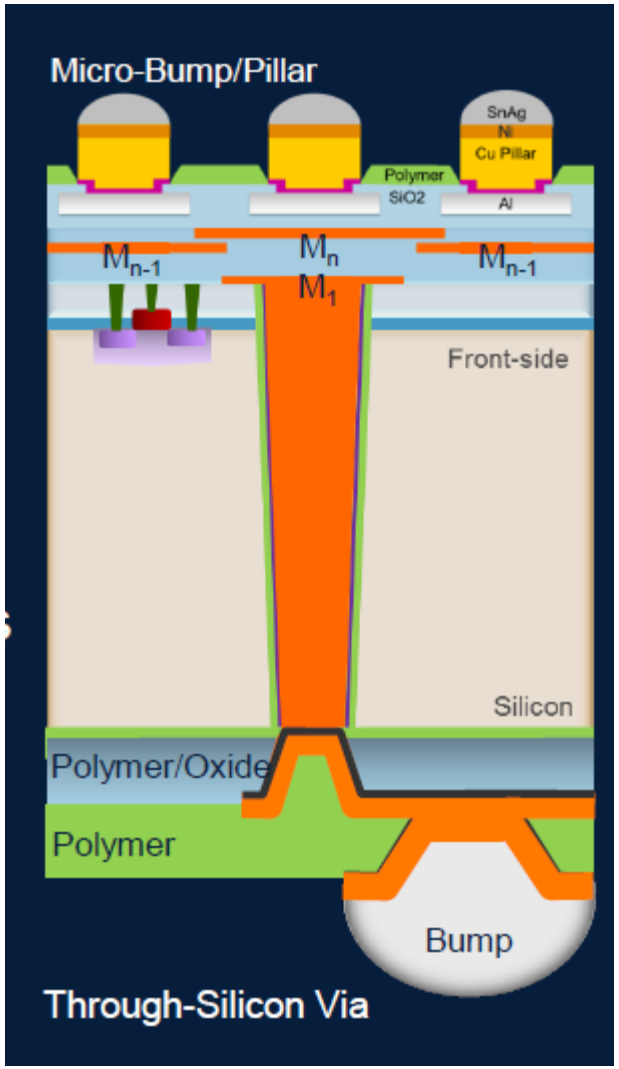
Introduction of Package

TSV(Through-Si Via) Process

TSV(through silicon via, 실리콘 관통전극)
- 와이어로 칩 연결하는 와이어 본딩(wire bonding) 대체
- 칩에 미세한 구멍(via)을 뚫어 상단 칩과 하단 칩을 전극으로 연결하는 패키징(packaging) 기술 (backside CMP 기술)
- 빠른 신호전달, 고용량, 저전력에 유리

- 2010년 삼성전사에서의 TSV 기반 D램 모듈 개발 발표
- 2013년 12월 26일 SK하이닉스에서 TSV 기술을 적용한 초고대역폭 메모리(HBM, high bandwidth memory) 개발

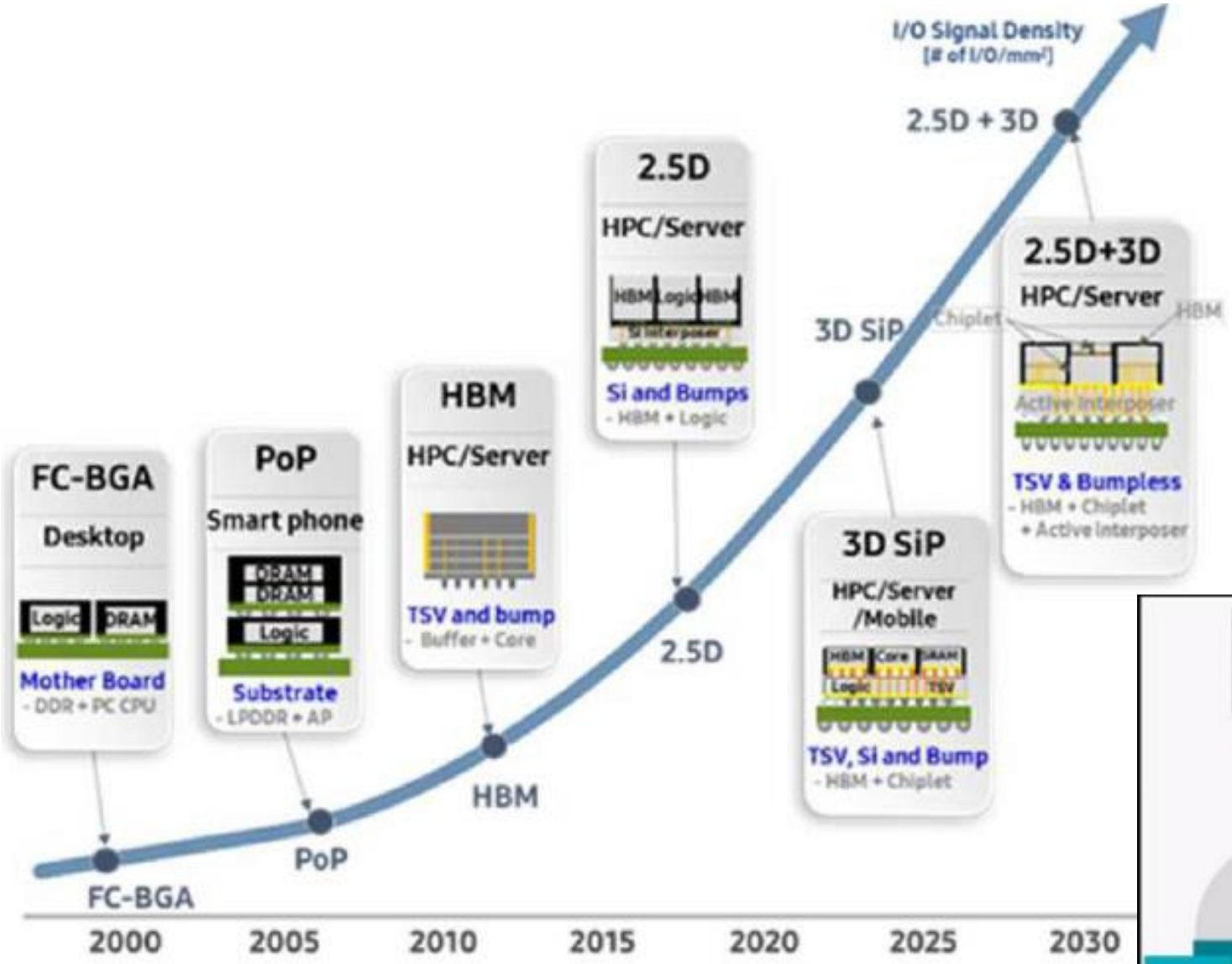


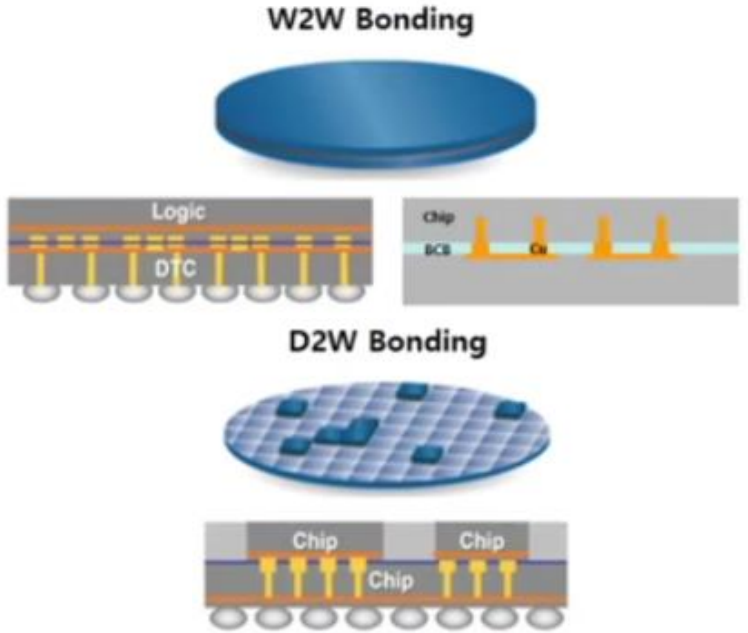


Source: applied materials

Introduction of Package

Advanced Package Roadmap (Foundry @IEDM2021 Samsung Keynote)





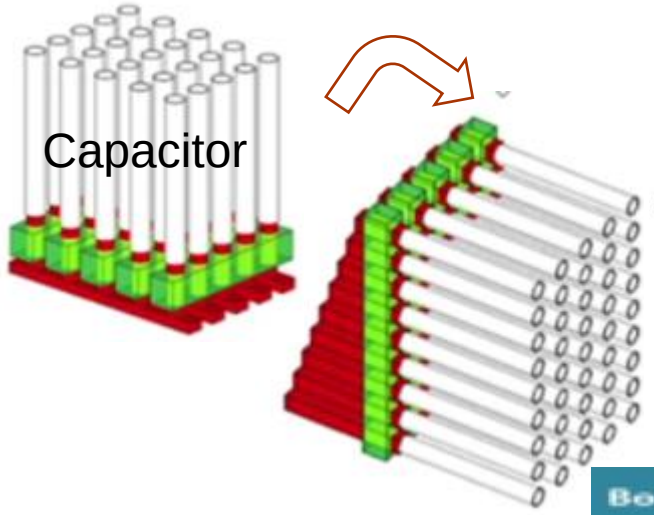
Source: SAFE2020, samsung

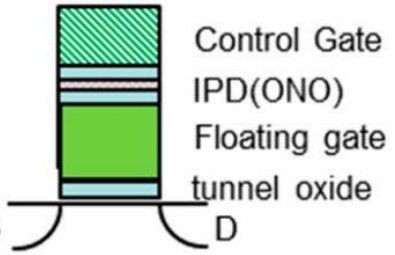
Summary - 3D structure (Architecture)

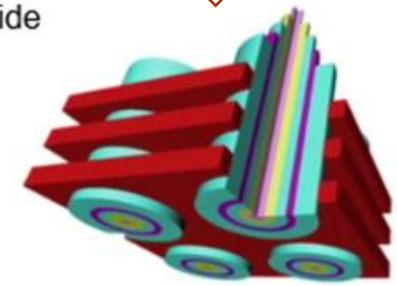
Cell 3D structure
Cell / Peri wafer backside Hybrid Bonding

DRAM	NAND	Logic(CPU, AP)

3D Cell

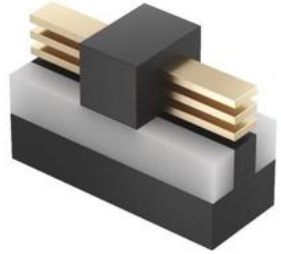




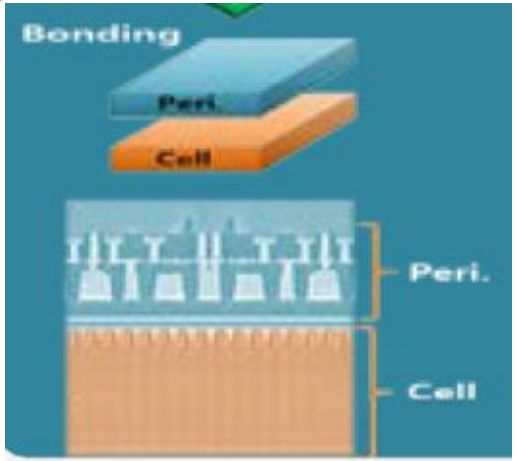


* IEEE 2019

FinFET



GAA



Backside Hybrid Bonding

BS-PDN (Power Via)

Summary - Key Technology

- **Patterning**
  - Photo: **EUV, Mask (Dry PR)**
  - Multi-patterning: **ALD(Atomic Layer Deposition)**
    ASD(Area Selective Deposition)
  - Dry Etch : **ALE(Atomic Layer Etch)**
  - High selective Etch : **Oxide/SiN (VNAND Mold stack)**
    Si/SiGe (Logic GAA stack, 3D DRAM Cell stack)

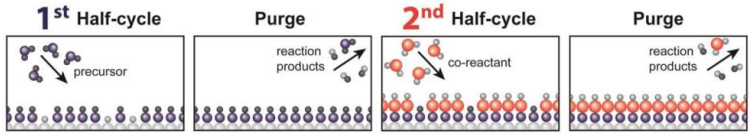
- **Thin Film(Metal & Dielectric)**
  - Dielectric: **low-k, Capacitor & Transistor (High-k, electrode)**
  - Metal: **Low resistivity (materials & Barrierless Metal, Co, Ru, Mo)**
    High Aspect Ratio (HAR) Gap-fill Metal (ALD-W, Mo)
  - BEOL: **Cu, Ru, Co**
    ALD, ASD (inhibitor) (ESL ALO)

- **3D : Hybrid bonding**

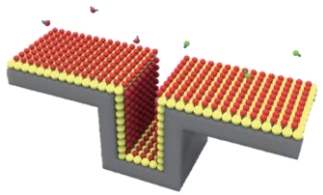
Summary - Key Technology

Atomic Layer Deposition (ALD)

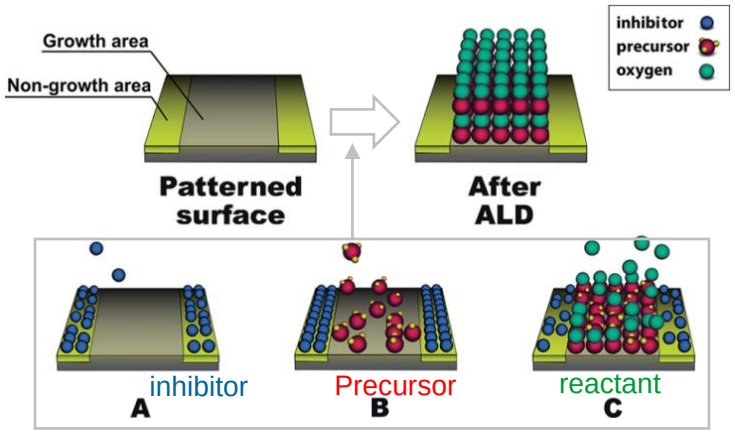
ALD Cycle



ALD Precursor

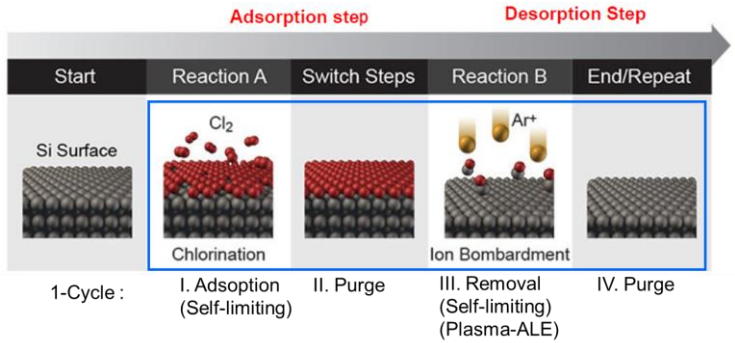


Area-selective ALD (ASD)



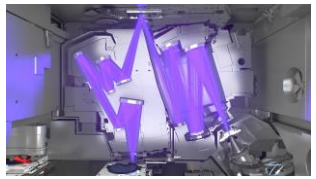
Area Selective ALD ABC-Type (w/ inhibitor)

Atomic Layer Etching (ALE)

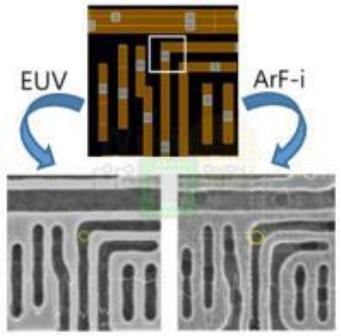


+ Cryogenic ALE (<90℃)
+ selective ALE (w/ inhibitor)
+ ALE Type Dry Cleaning(ALC)

High NA-EUV



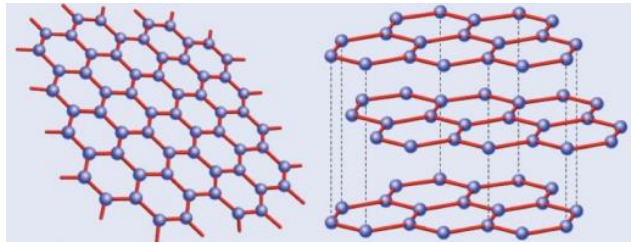
λ=13.5nm



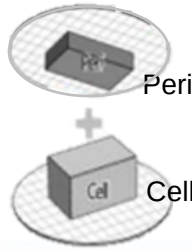
N.A 0.55
Co2 laser
Tin droplet
Mirror
Reticle & pellicle
Turbo Molecular Pump (CxHy outgassing)

2D Materials

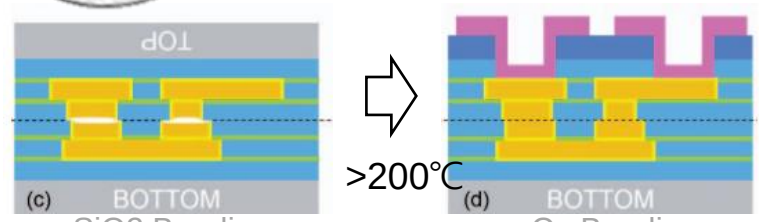
(1) PECVD-Graphene
(2) MoS2, MoSe2, MoTe2, WS2, etc



Hybrid Bonding



CTE (Coefficient of Thermal Expansion)	PECVD SiO2	Cu
	4.4×10^{-6}/°C	16.6×10^{-6}/°C



SiO2 Bonding

Cu Bonding

Leading the World

In Vacuum Technology

ULVAC