Dream
Design
Discover
Explore
Experience

반도체 Nanoscale-down을 위한 원자층 증착 기술

'Atomic Layer Deposition for Nano-scale Semiconductor Application'

2022. 11. 11

Division of Materials Science and Engineering
Hanyang University
Prof. Jin-Seong Park

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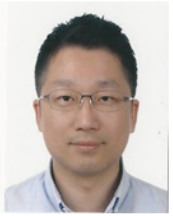
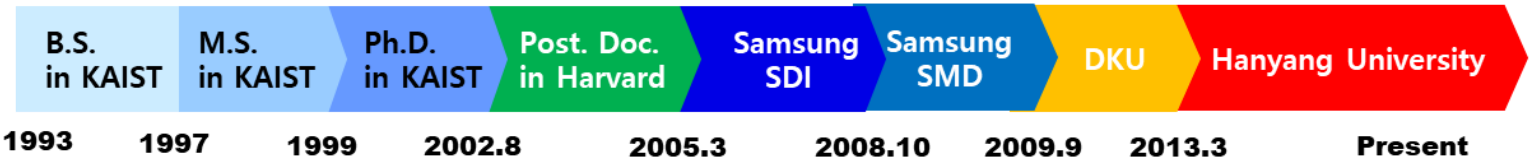
■ Education & Career Background





'97.3~'99.2 Master degree in Materials Science and Engineering (**KAIST**)

-Thesis: A study of the deposition model about Atomic layer deposition TiN method (Prof. Sang-Won Kang)

'99.3~'02.8 Ph. D. in Materials Science and Engineering (KAIST)

-Ph. D. in the Semester (Age: 26 years 8 months old), Making PEALD Tool with Genitech (現ASM)

-Thesis: A study on the **plasma enhanced atomic layer deposition** of Ta-N, Ti-N and Ti-Si-N thin films

'03.1~'05.1 Post Doc. in Chemistry and Chemical Biology **(Harvard University, Prof. Roy G. Gordon)**

- Synthesizing and developing Electronic materials
- Metal, Oxide, Nitride Thin Films with Amidinate precursors, ALD Tool Maker

'05.3~'08.9 Senior Engineer in R&D center (Samsung SDI)

- **Oxide TFT Project Initiator, Advanced Thin Film Transistor for AMOLED (Oxide semiconductor)**

'08.10~'09.8 Senior Engineer in R&D center (Samsung Mobile Display)

- **(Flexible) Oxide TFT team PA leader & A Chief Secretary in Samsung Group-Oxide TFT Research Assoc.**

'09.9~13.2 Assistant Prof. MSE, Dankook University
'13.2~17.2 Associate Prof. MSE, Hanyang University (Seoul)
'17.3~Present Full Professor, MSE, Hanyang University (Seoul)

Prof. Jin-Seong Park @ Hanyang Universtiy

Research Activity

- Semiconductor/Display materials and device, (Plasma Enhance) Atomic Layer Deposition (Precursor, Tool, Process)
- Oxide TFTs and Device Physics: defect analysis and Mechanical degradation mechanism
- High mobility InGaZnO ALD, HQ SiO_2 & SiNx ALD. Sub-nm level Molecular Layer Deposition Patterning Process & Area Selective Atomic Layer Deposition
- Korean Information Display Society (KIDS), Planning Secretary since 2010

Korean Material Research Society (K-MRS, Secretary), Electronic Material Letters (SCIE, Editorial Board)

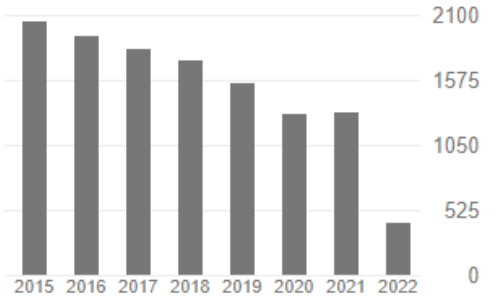
American Vacuum Society (AVS) Thin Film Division Member, International ALD committee member

Publication (over 250 SCI Papers, over 100 patents) & Total Citation : > 18500 hits

☐ **Achievement & Research statistics**

1. **Merck Young Scientist Award (2014) & Merck Special Award (2021)**
   "**Oxide TFT Material, Process, and Mass-production**""
2. **Korea Evaluation Institute of Industry Technology, President Award (2017)**
   : **A Leading Researcher on Flexible Thin Film Device Applications**
3. **International Conference (Award, Tutorial, Invited Speakers)**
   -IMID, SID Best & Distinguished Papers
   -IMID 2014 & Korean Physics Society, Oxide TFT Tutorial Speaker
   -ALD Conference, AVS64, Invited Speaker for Flexible Display
4. **18th International Atomic Layer Deposition Conference**
   : **General Chair** (American Vacuum Society, 2018. Songdo-Incheon)

	전체	2017년 이후
서지정보	18458	8187
h-index	53	42
i10-index	169	135



(Source: Google Scholar)

History of Atomic Layer Deposition

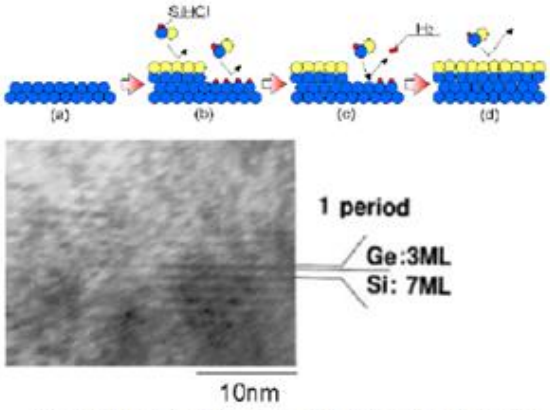
1970s

- T. Sultola developed the concept of ALD [US patent 4 058 430 (1977)] and named it Atomic Layer Epitaxy

- Thin Film Electroluminescent (TFEL) flat panel display manufactured
  : $Al_2O_3/ZnS:Mn/Al_2O_3$ Structure

Mid-1980 ~ Mid-1990

- Research focused on the epitaxial growth of III-V, II-IV, Si, and Ge using ALD



Ref: Journal of the Korean Physical Society, 30, 447 (2001)

Name

ALE (Atomic Layer Epitaxy)
→ The original name, but for eptaxial films only

ALCVD (Atomic Layer CVD)
→ Emphasizes the relation to CVD

ALD (Atomic Layer Deposition)
→ General, covers all kinds of films

Beginning of the 21th Century

- ALD process was adopted for semiconductor device scaling

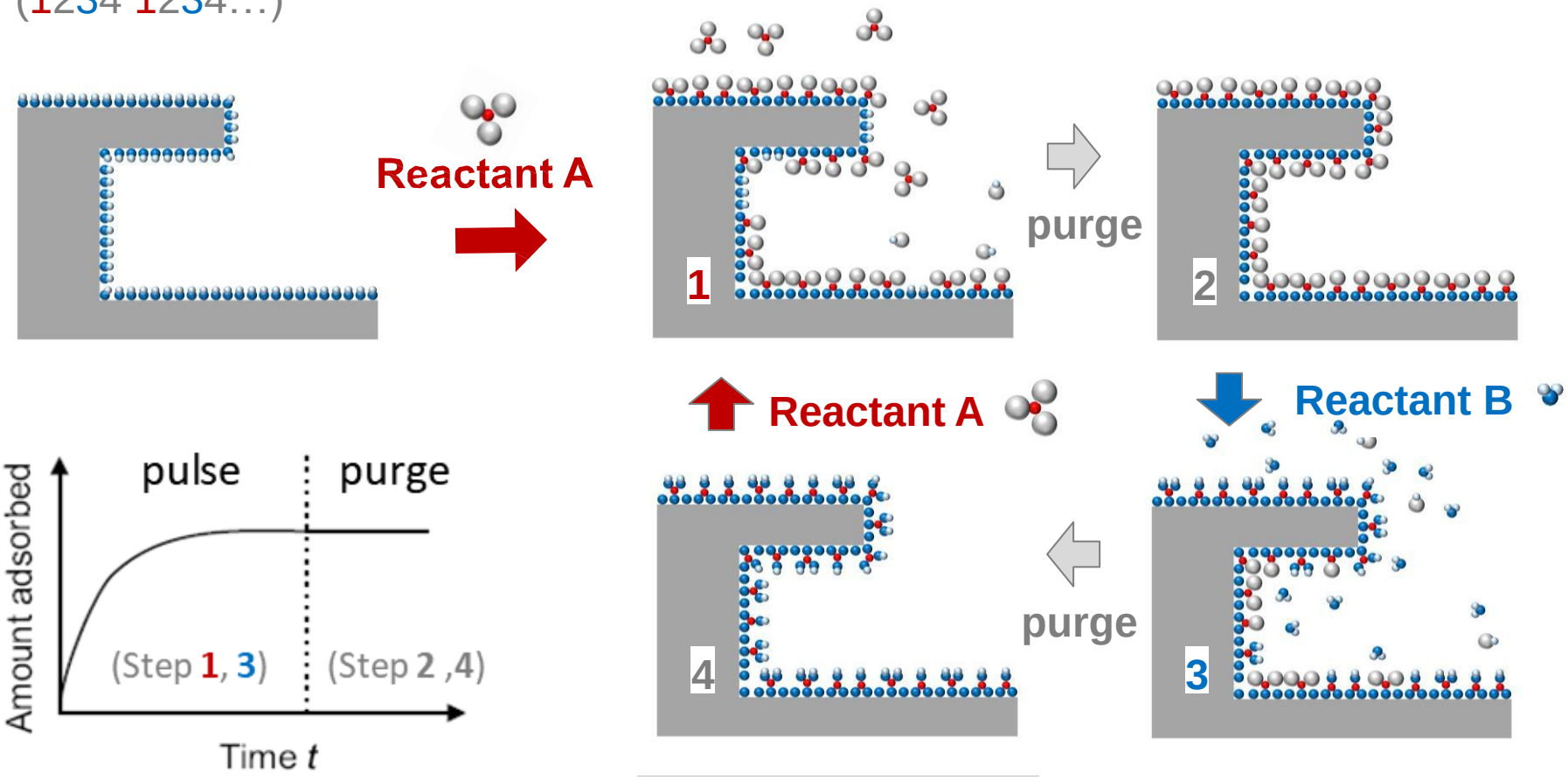
1st application
: Apply Al_2O_3 to DRAM capacitor

In 2007
: Intel announced applying ALD HfO_2 to CMOS Tr.

Atomic Layer Deposition

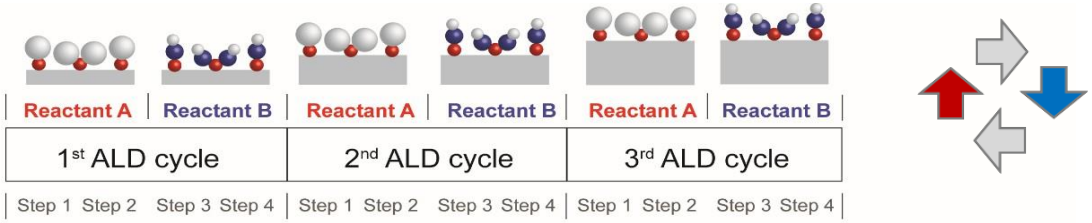
A B A B…

(1234 1234…)

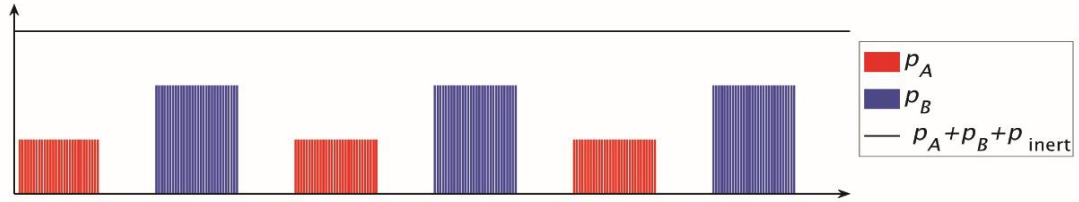


Aristeidis Goulas, Riikka L. Puurunen, J. Ruud van Ommen, 2020, Wikimedia Commons, CC BY 4.0, link; ALD-cartoons-evolving-file
Riikka Puurunen, Fundamental of ALD, ALD 2021 Tutorial

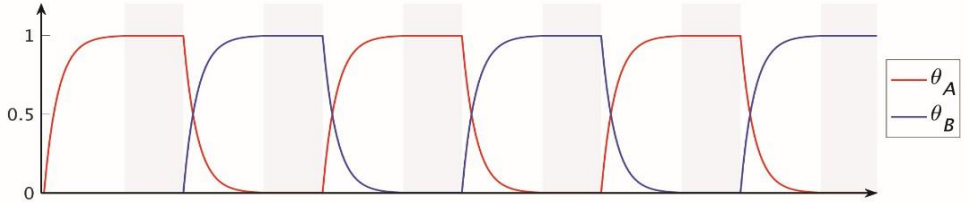
Atomic Layer Deposition



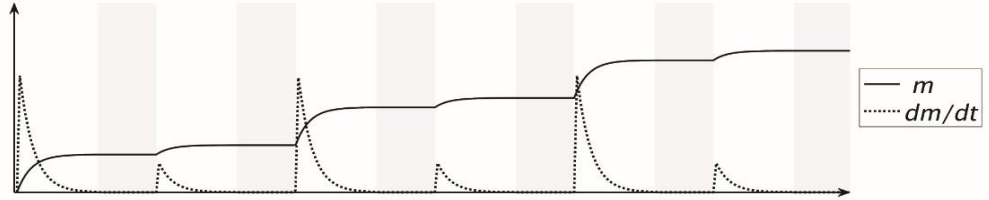
Partial pressure
Reactant A
Reactant B

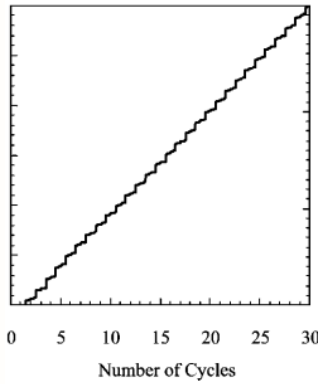


Surface coverage ($0 \le \theta \le 1$)
From Reactant A
From Reactant B



Mass adsorbed



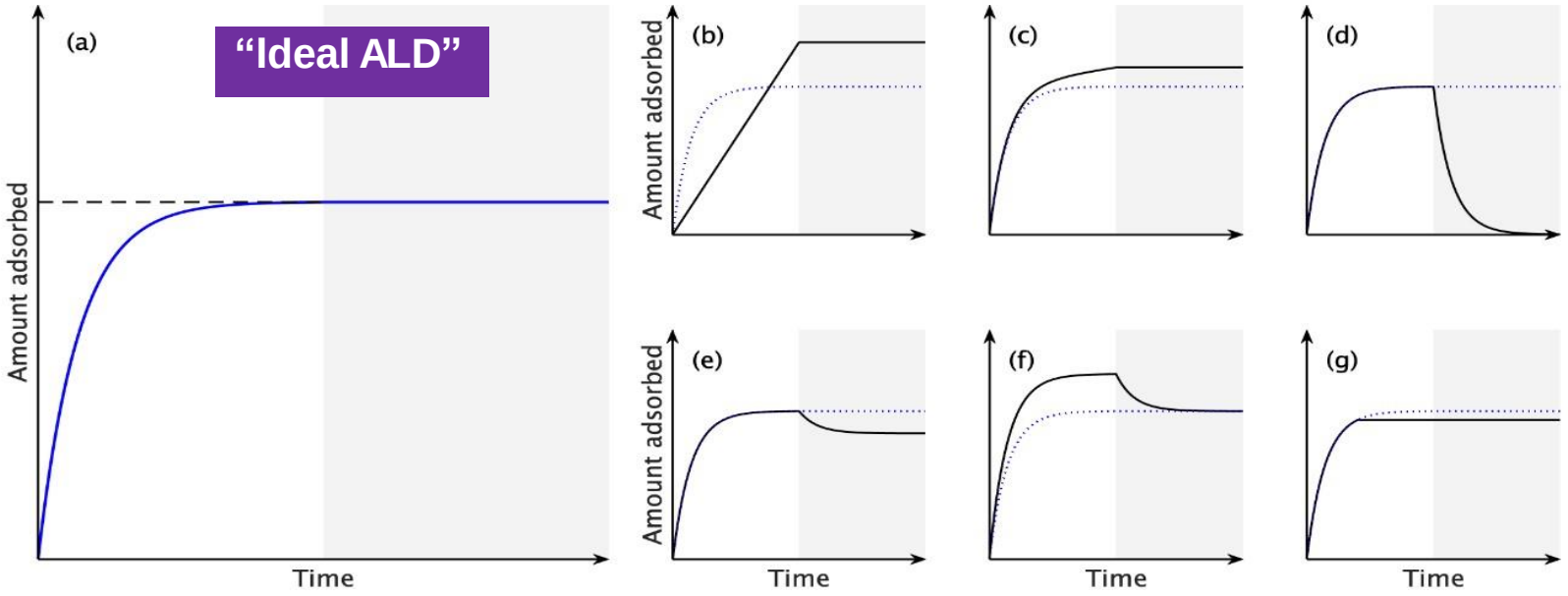


George, Chem. Rev. 110 (2010) 111.
DOI: 10.1021/cr900056b

J.R. van Ommen, A. Goulas, R.L. Puurunen, Kirk-Othmer Encyclopedia of Chemical Technology, in press (2021).
Adapted from Puurunen, J. Appl. Phys. 97 (2005) 121301, https://doi.org/10.1063/1.1940727
https://commons.wikimedia.org/wiki/Category:Atomic_layer_deposition#/media/File:Schematic_illustration_of_changes_with_time_during_three_ALD_reaction_cycles.png

Atomic Layer Deposition

ALD: saturating, irreversible reactions



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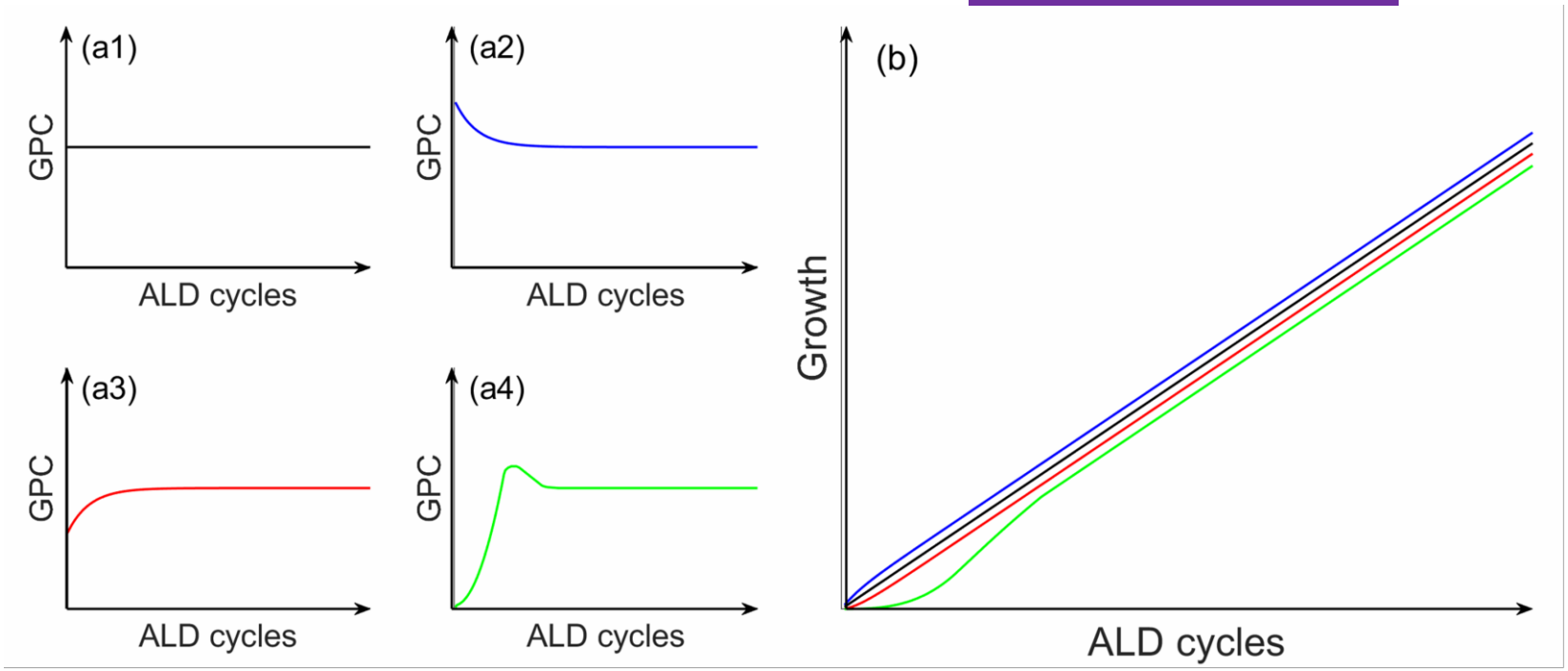
Adapted from Puurunen, J. Appl. Phys. 97 (2005) 121301, https://doi.org/10.1063/1.1940727
https://commons.wikimedia.org/wiki/Category:Atomic_layer_deposition#/media/File:Various_dependencies_for_adsorption_vs._time_in_ALD_and_other_cases.png

Atomic Layer Deposition

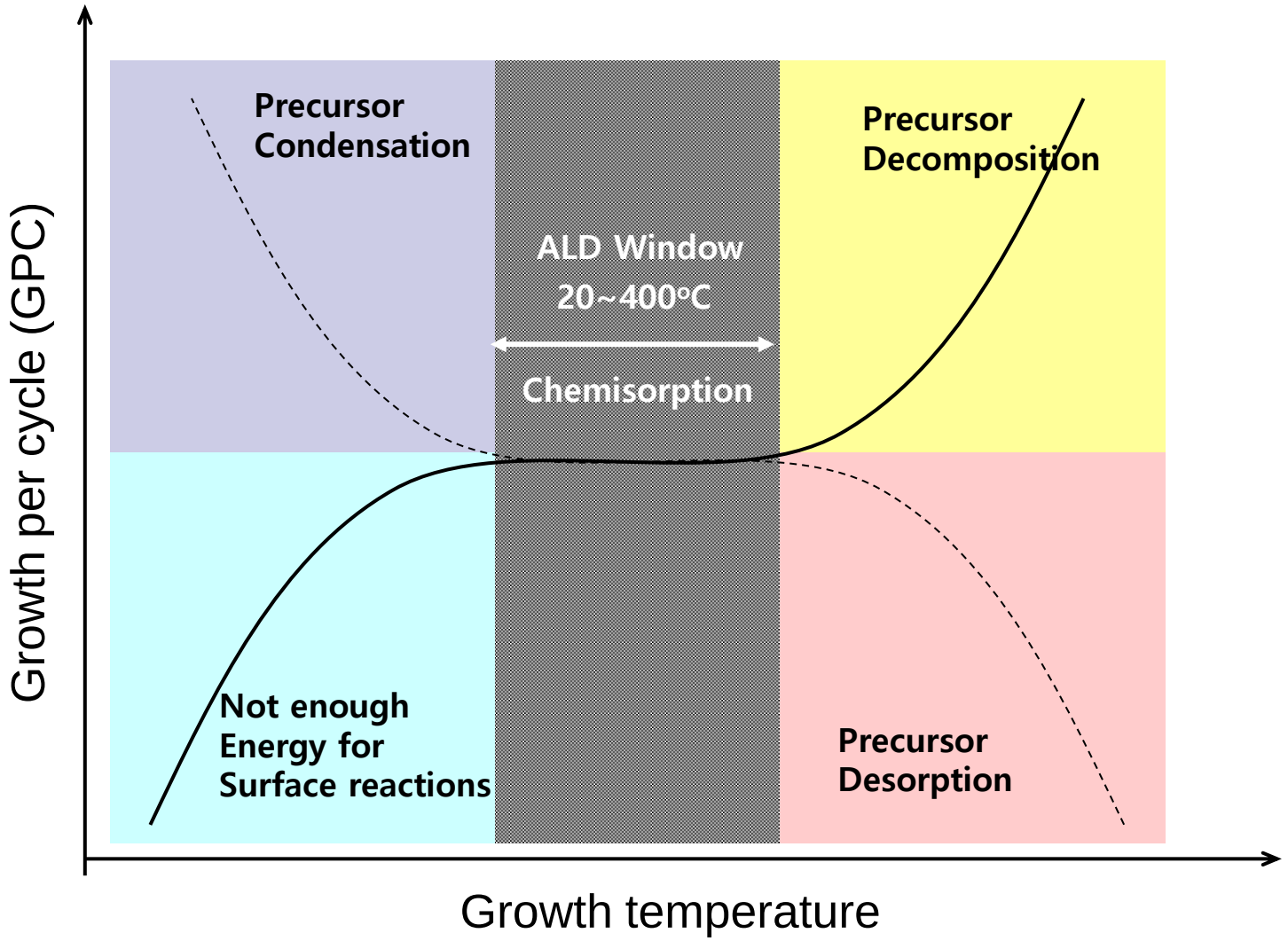
Growth vs. cycles

"growth curve"

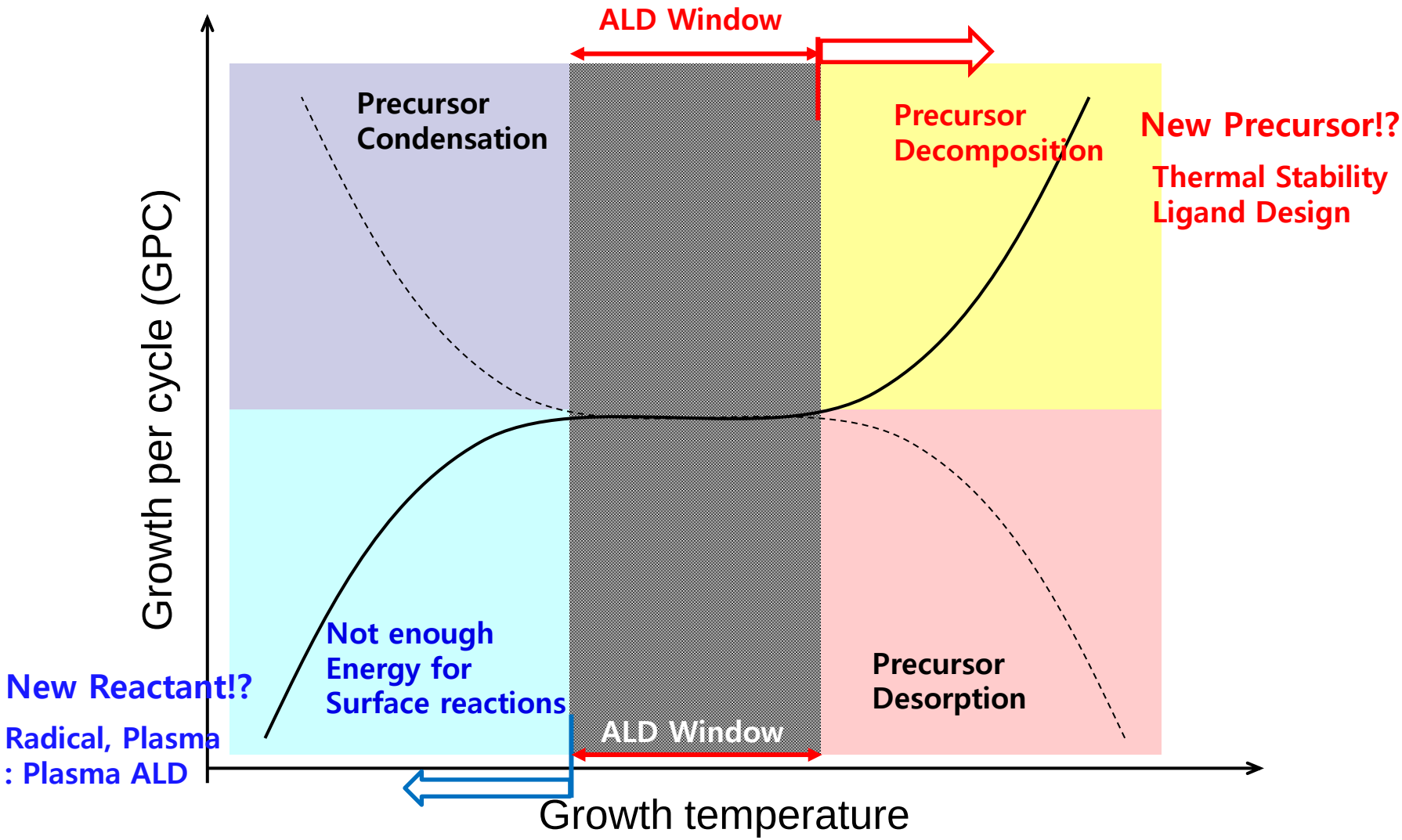


Adapted from: Puurunen, J. Appl. Phys. 97 (2005) 121301. DOI: 10.1063/1.1940727
J.R. van Ommen, A. Goulas, R.L. Puurunen, Kirk-Othmer Encyclopedia of Chemical Technology, in press (2021).
https://commons.wikimedia.org/wiki/Category:Atomic_layer_deposition#/media/File:Ways_the_GPC_in_ALD_can_vary_with_cycles.png

Atomic Layer Deposition (GPC vs. Temperature)



Atomic Layer Deposition (GPC vs. Temperature)



Atomic Layer Deposition : Precursor

■ Organometallic compounds, Inorganic metals compounds

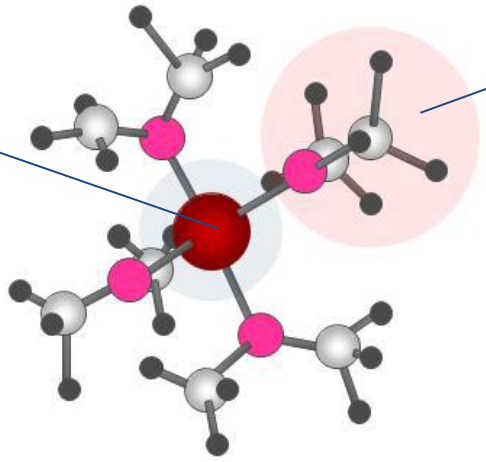
(ex. $AlMe_3$, $Ti(NMe_2)_4$, $TiCl_4$, $Ru_3(Co)_{12}$)

Should be stayed

Metallic center: TARGET

Should be removed

Ligand: VECTOR



Enabling metal supply
Enabling metal vaporization
Enabling ALD reaction

Atomic Layer Deposition : Precursor

☐ The versatility of CVD and ALD ultimately rests on the behavior and reactivity of the precursor used.

☐ This design can be guided by a short list of target properties, namely a low melting point, high volatility and thermal stability, and high, self-limiting reactivity.

☐ A low melting point is ideal, and this is most achieved by designing ligands with branched moieties that frustrate crystallization.

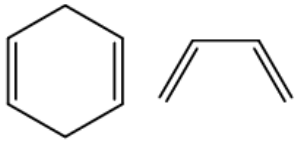
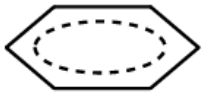
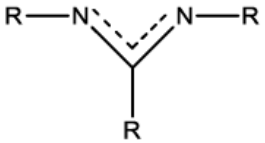
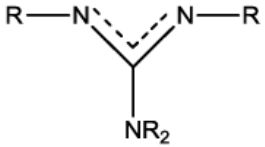
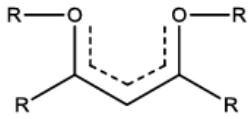
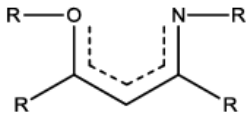
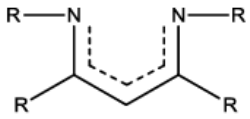
☐ Volatility must be well characterized to establish suitability for CVD/ALD and to inform process parameters.

☐ Stability must be balanced such that transport to the surface is possible and reaction at the surface is likely.

☐ Reactivity must occur at the surface and no sooner, with the further constraint that in ALD the resulting surface species eliminates all routes for further chemisorption of that precursor.

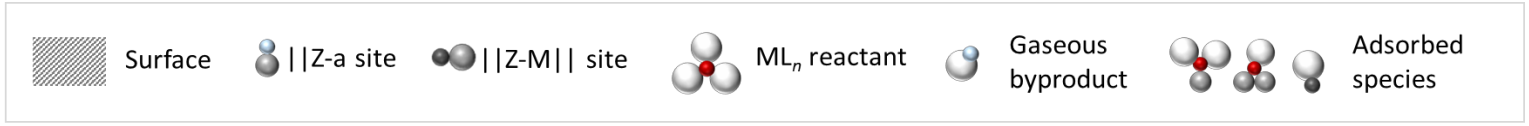
Atomic Layer Deposition : Precursor

■ Frequent Ligands for ALD Chemistry

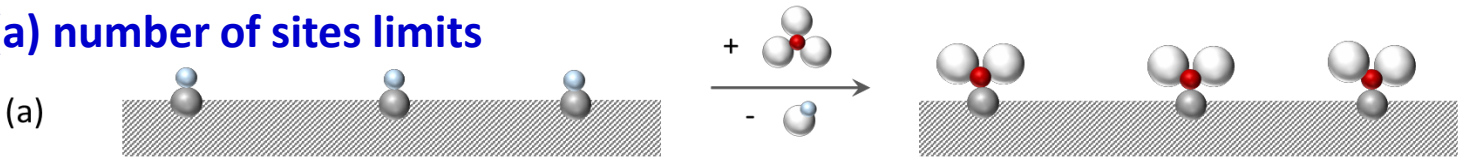
X Halogen	R Alkyl	OR Alkoxide	NR_2 Alkylamido	NR Imido	SiR_3 Alkylsylil	CO Carbonyl	CR_2 Carben
 Dienyl	 Arene	 Allyl	 Amidinate	 Guanidinato			
 Acac β–diketonato	 AcNac (Ketiminato)	 NacNac (Diketiminato)	 Cyclopentadienyl	PR_3 Phosphine			

R = alkyl group

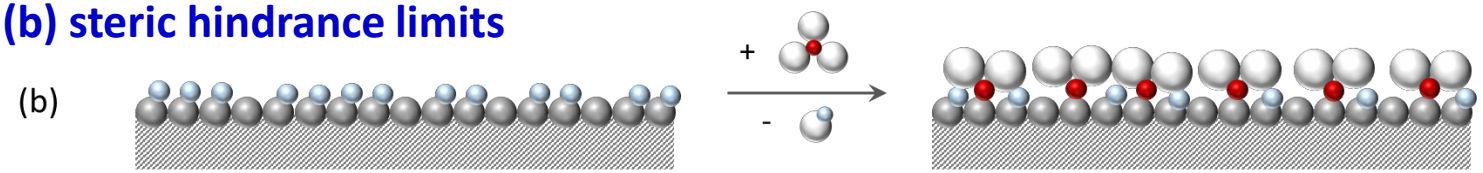
Atomic Layer Deposition : Surface Coverage & Selectivity



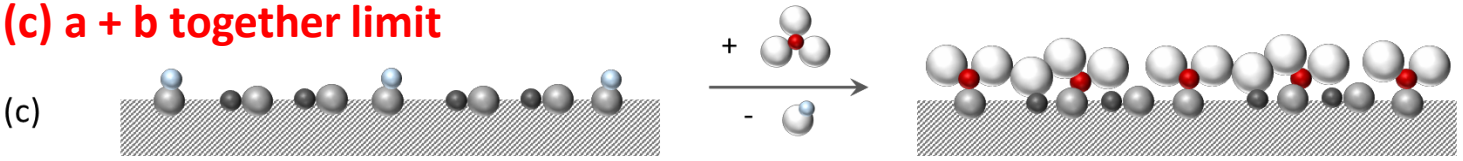
(a) number of sites limits

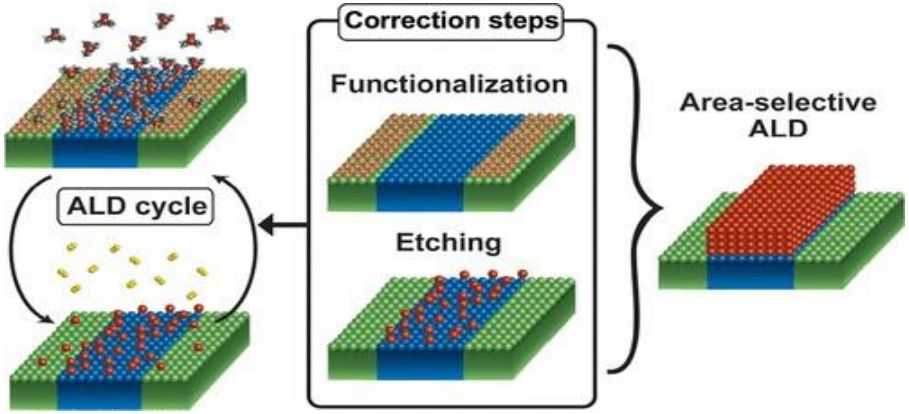


(b) steric hindrance limits



(c) a + b together limit



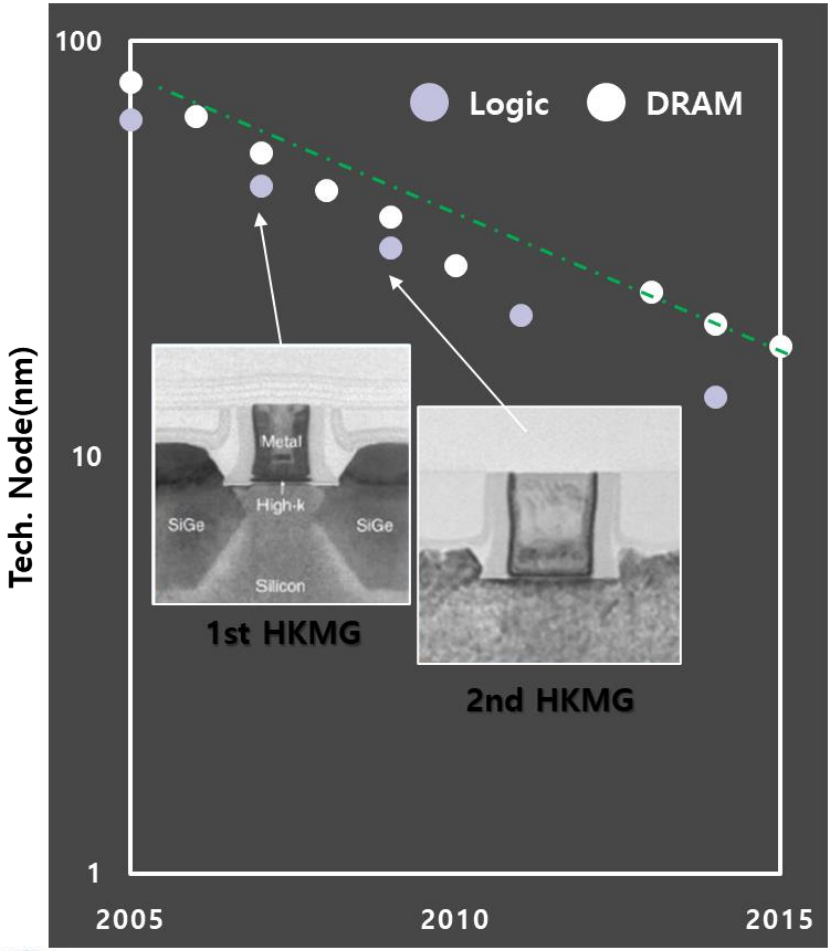


Puurunen, J. Appl. Phys. 97 (2005) 121301
Mackus. Merkx, Kessels, Chem. Mater. 2019, 31, 1, 2–12

New Challenges for scale-down

High-k & Metal Gate

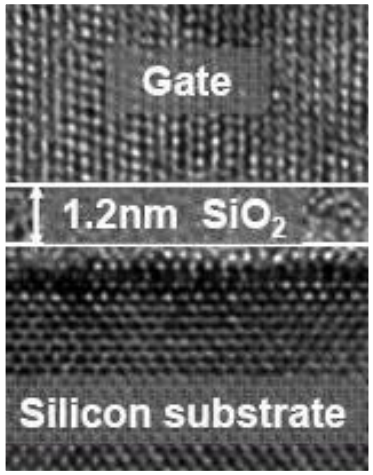
High-k /metal gate technology is necessary for the sake of reducing EOT (Equivalent Oxide Thickness).

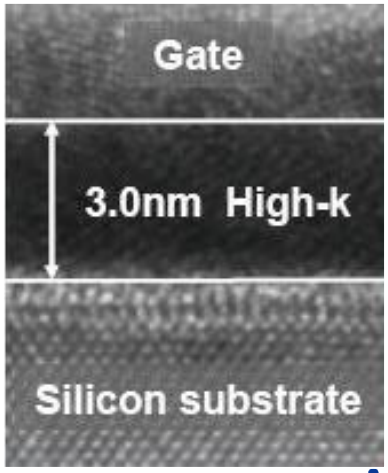


$$t_{eq} = \frac{k_{OX}}{K \times t_{phys}} \qquad I_D \propto g_m \propto \frac{k}{t_{phys}}$$

Dielectric constant (k)
Silicon oxide ~ 3.8
ZrO2/Al2O3/ZrO2 ~ 40

Higher Thickness → Gate leakage reduction

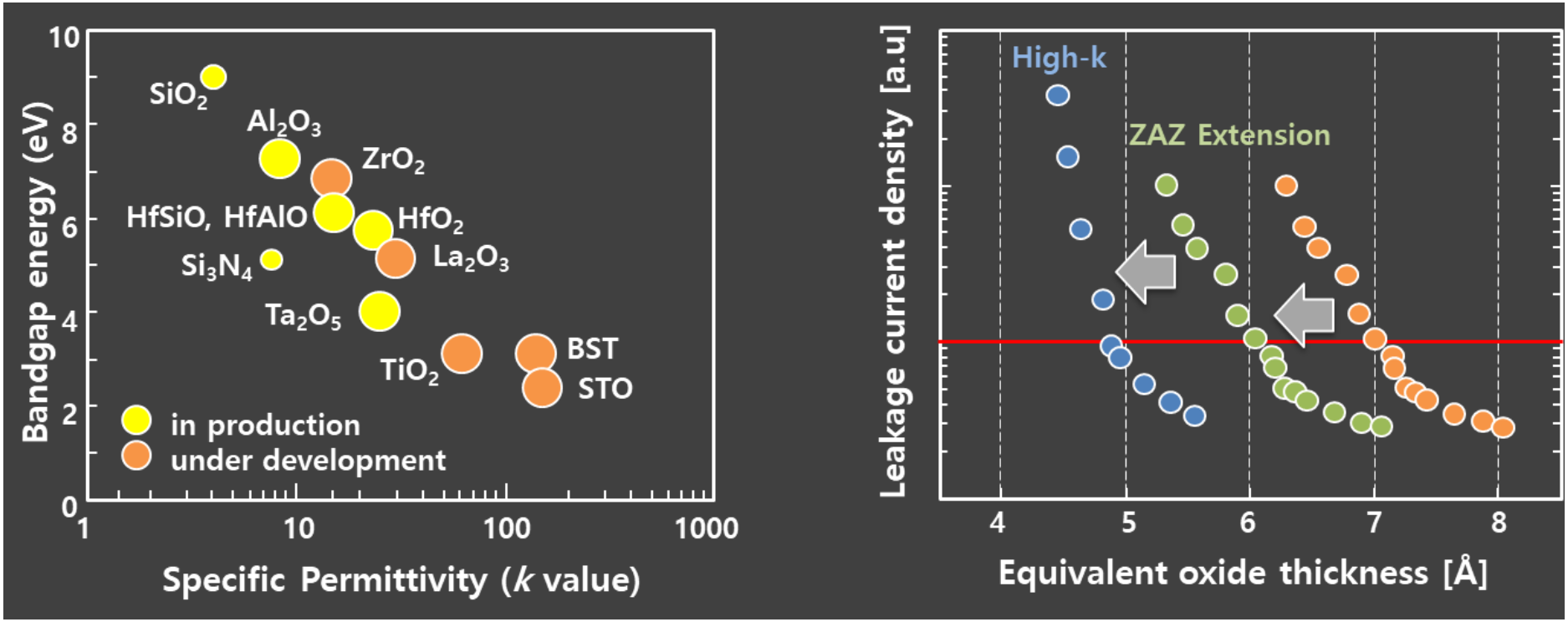




New Challenges for scale-down

High-k Capacitor Dielectrics

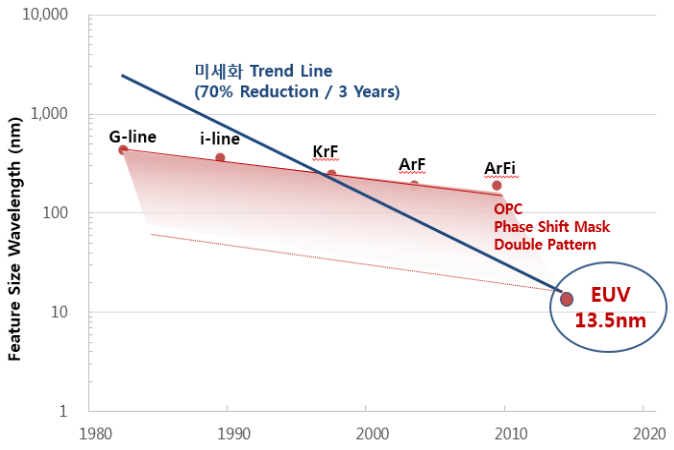
Trade-off between bandgap energy and permittivity of high-k dielectric.



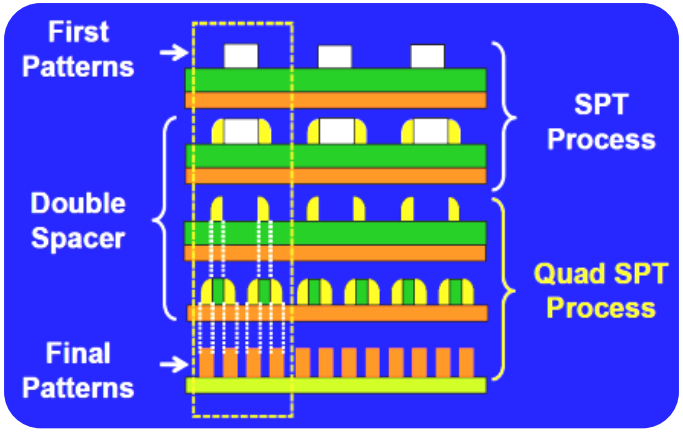
New Challenges for scale-down

Lithography

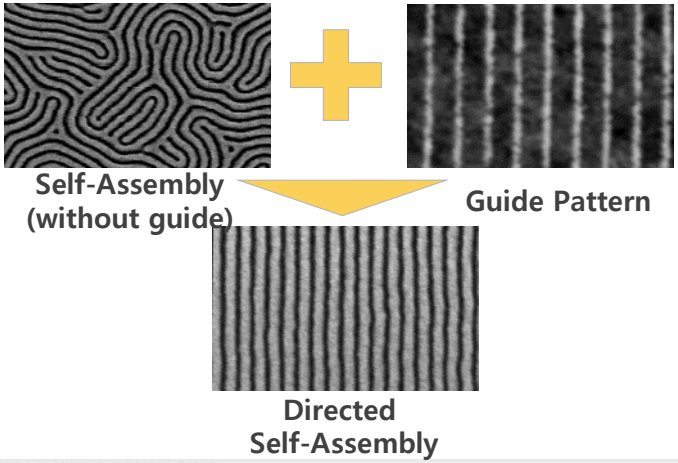
EUV(Extreme UV, 13.5nm)



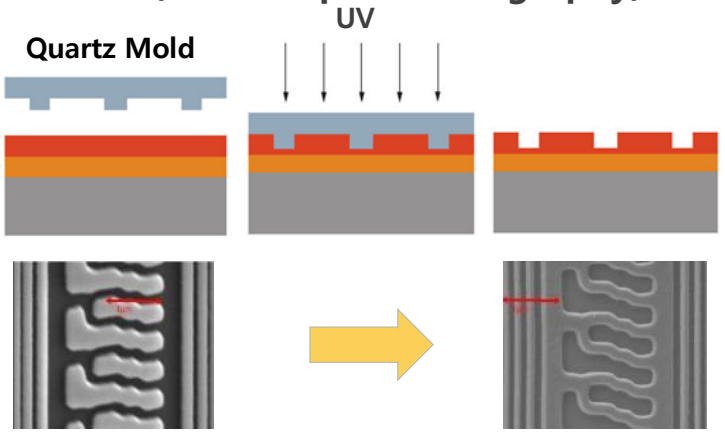
Quadrupole Patterning



DSA(Directed Self Assembly)



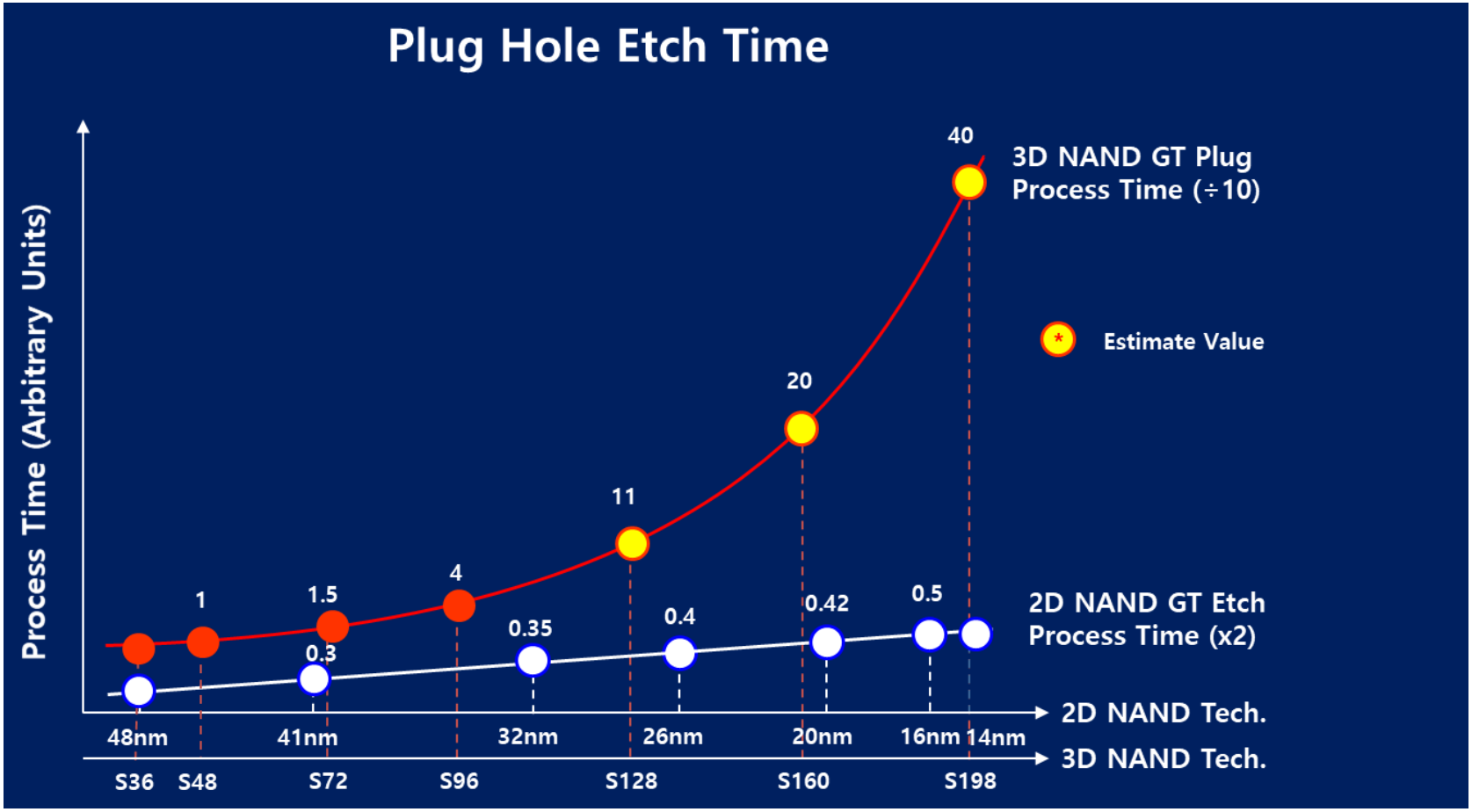
NIL(Nano Imprint Lithography)



New Challenges for scale-down

3D NAND Stack-Up Issues

As 3D NAND Stacks up, it is necessary to overcome Throughput Reduction and Equipment Variation.



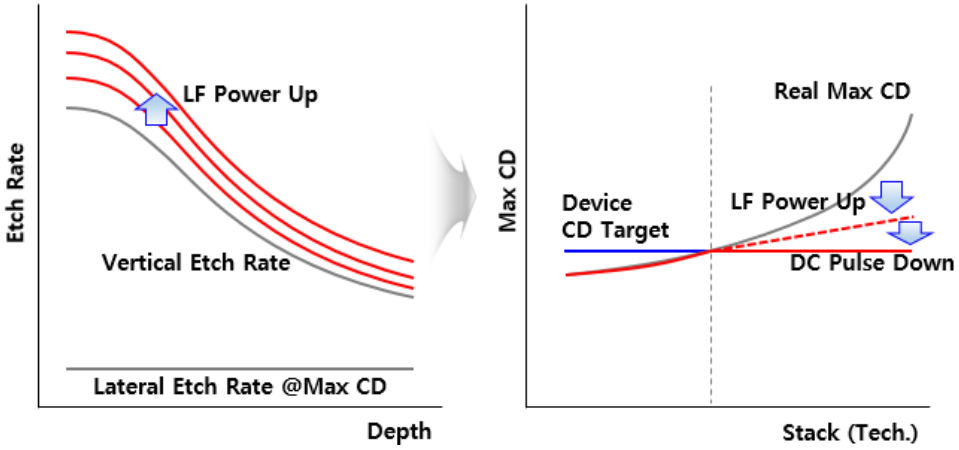
New Challenges for scale-down

High Aspect Ratio Contact (HARC) Etch

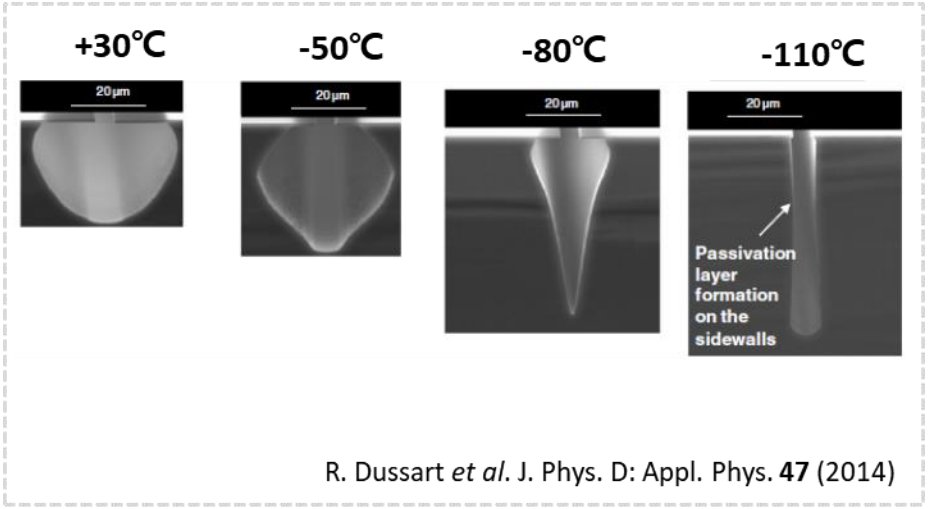
Continuous LF Power-up and shorter Duty Pulsing Cycle for HARC Etch

Cryogenic Etcher : High Selectivity & High Etch Rate, more less Necking & Clogging

[LF Power Up and Duty Cycle Down]



[Temp. Dependence on Si Etching with SF_6/O_2]



R. Dussart *et al.* J. Phys. D: Appl. Phys. **47** (2014)

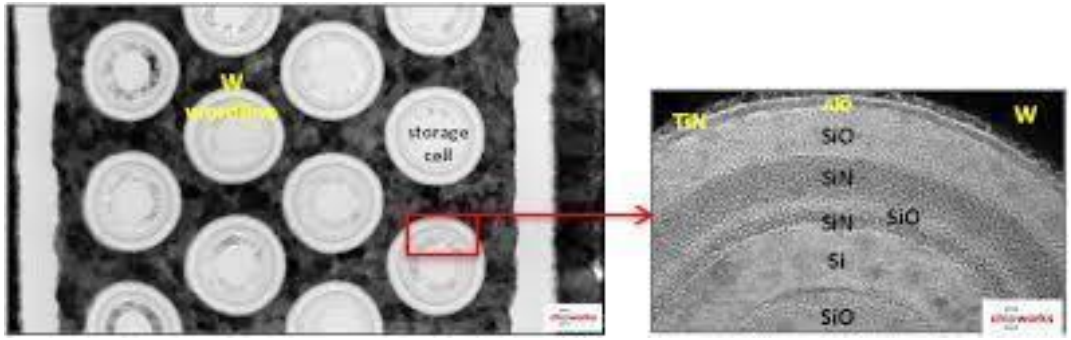
○ Improved Necking & Clogging Phenomenon by low temp Etch

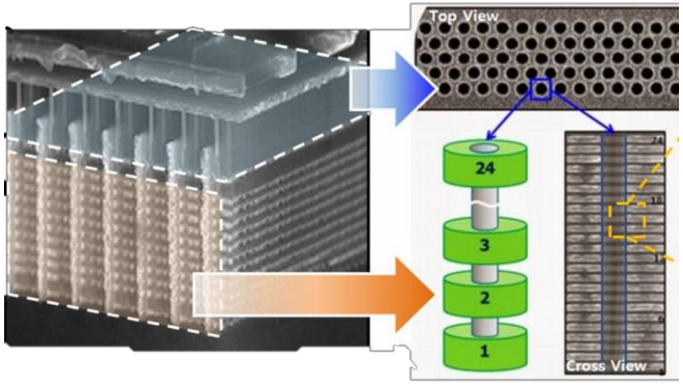
New Challenges for scale-down

Metal Interconnection (WL)

. More than 30% low stress of CVD W

. More than 10 times low F concentration in the W film





. Have to consider an effect of Electron Mean Free Path on the resistivity

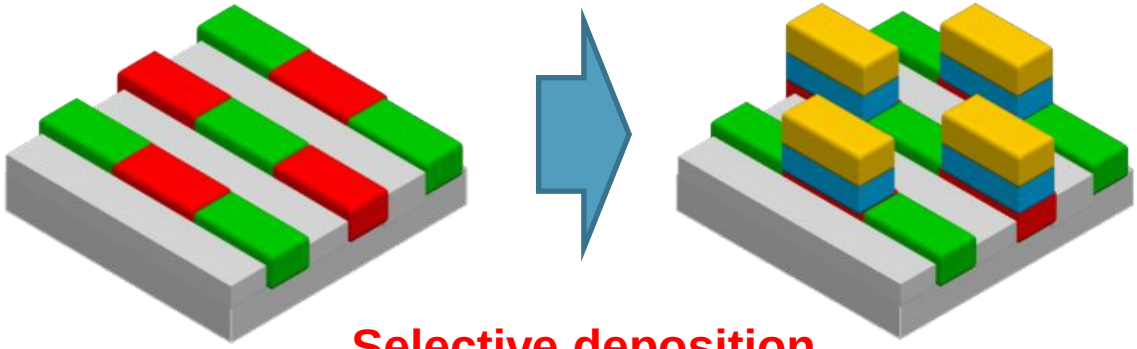
Element		Crystal structures	$\rho_{o,n}$ ($\mu\Omega$ cm)	v_f (10^5 m/s)	$\tau \times \rho_o$ (10^{-22} Ω m s)	$\lambda \times \rho_o$ (10^{-16} Ω m^2)	τ_n (fs)	λ_n (nm)
Silver	Ag	fcc	1.587	14.48	5.84	8.46	36.8	53.3
Copper	Cu	fcc	1.678	11.09	6.04	6.70	36.0	39.9
Gold	Au	fcc	2.214	13.82	6.04	8.35	27.3	37.7
Aluminum	Al	fcc	2.650	15.99	3.13	5.01	11.8	18.9
Calcium	Ca	fcc	3.36	4.80	24.7	11.9	73.6	35.4
Beryllium	Be	hcp	3.56	12.62	13.2/21.0	17.1/24.3	37.0/59.1	48.0/68.2
Magnesium	Mg	hcp	4.39	11.63	8.60/7.30	9.81/8.80	19.6/16.6	22.3/20.0
Rhodium	Rh	fcc	4.7	6.67	4.85	3.23	10.3	6.88
Sodium	Na	bcc	4.77	10.21	14.4	14.7	30.2	30.9
Iridium	Ir	fcc	5.2	8.54	4.32	3.69	8.30	7.09
Tungsten	W	bcc	5.28	9.71	8.44	8.20	16.0	15.5
Molybdenum	Mo	bcc	5.34	9.18	6.53	5.99	12.2	11.2
Zinc	Zn	hcp	5.90	15.66	6.80/4.90	10.3/8.1	11.5/8.31	17.4/13.7
Cobalt	Co	hcp	6.2	2.55	13.1/10.9	7.31/4.82	21.2/17.6	11.8/7.77
Nickel	Ni	fcc	6.93	2.34	10.0	4.07	14.5	5.87
Potassium	K	bcc	7.20	7.94	28.6	22.7	39.7	31.5
Cadmium	Cd	hcp	7.5	15.55	8.35/6.89	12.6/11.3	11.1/9.18	16.8/15.1
Ruthenium	Ru	hcp	7.8	7.24	6.88/5.51	5.14/3.81	8.82/7.07	6.59/4.88
Indium	In	bct	8.8	16.32	4.64/4.45	7.62/7.18	5.27/5.05	8.65/8.16
Osmium	Os	hcp	8.9	8.19	7.60/5.51	6.41/4.33	8.54/6.19	7.20/4.87

For a few nm scale
W, Co → Mo, Ru

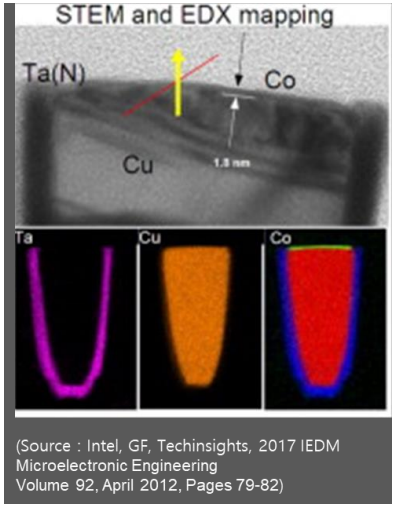
https://www.semanticscholar.org/paper/Electron-mean-free-path-in-elemental-metals-Gall/5fde93380cf4f2b5564c042d34b5610be16d18c3

New Challenges for scale-down

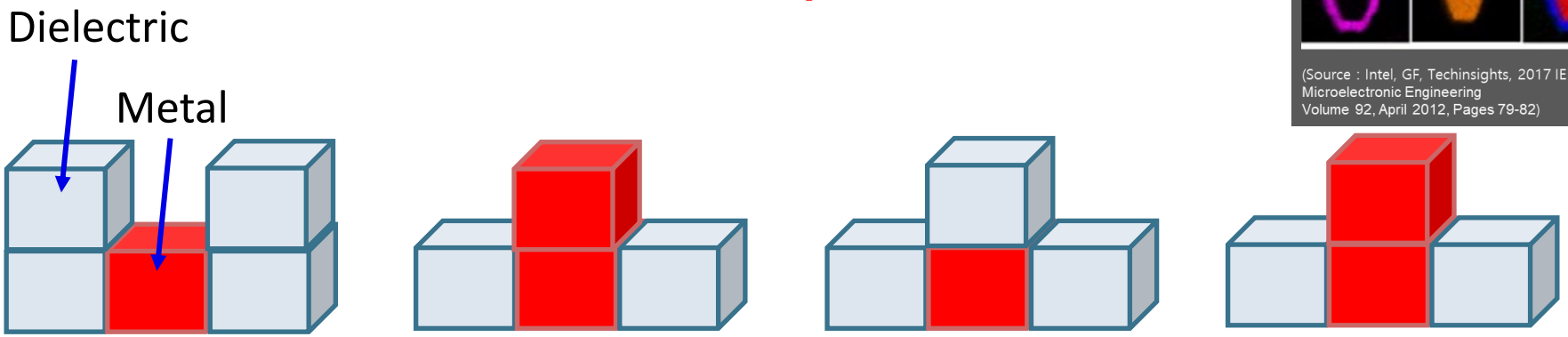
Area Selective Deposition (ASD)



Selective deposition



(Source : Intel, GF, Techinsights, 2017 IEDM
Microelectronic Engineering
Volume 92, April 2012, Pages 79-82)



dielectric on dielectric

dielectric on metal

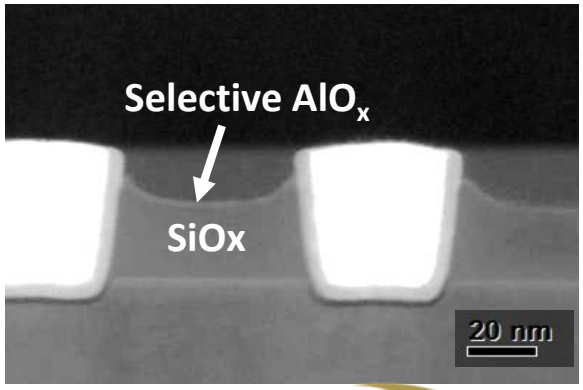
metal on dielectric

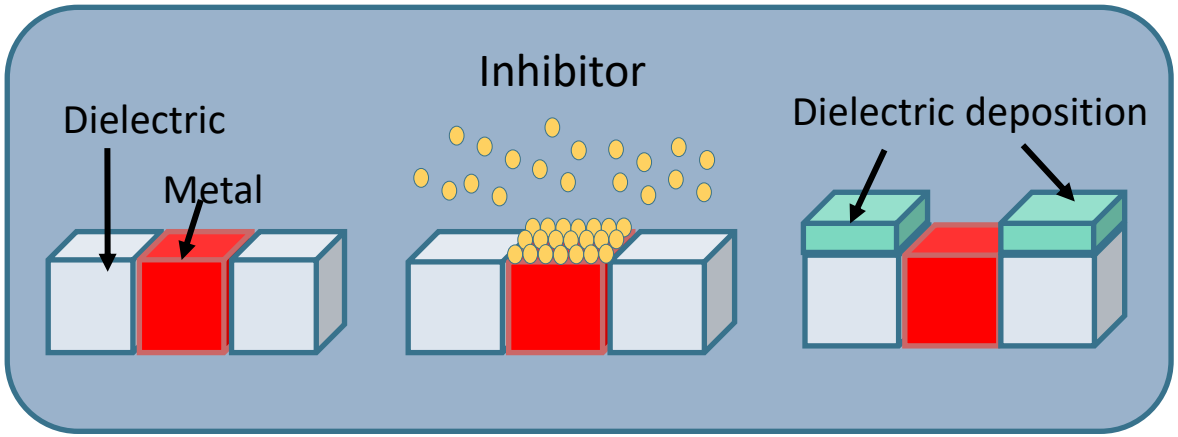
metal on metal

New Challenges for scale-down

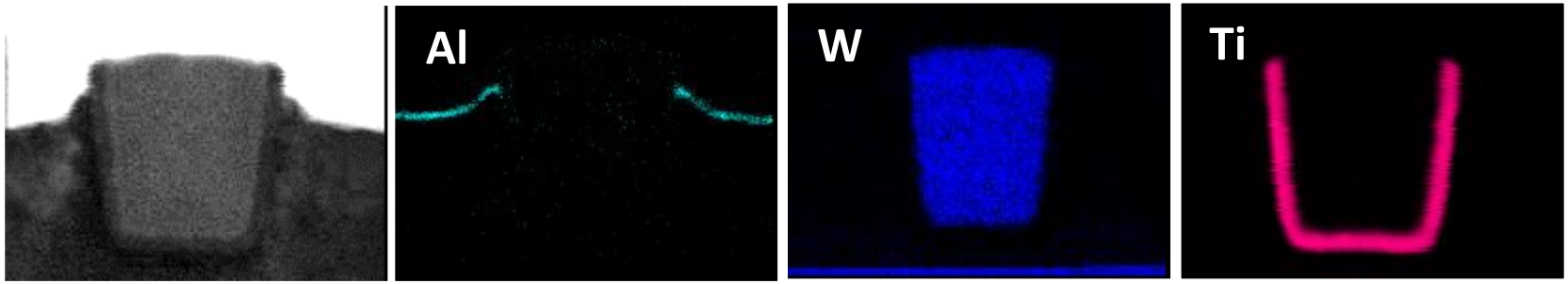
Area Selective Deposition (ASD)

❖ ASD of AlO_x on dielectric





▪ EELS Analysis

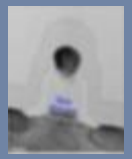
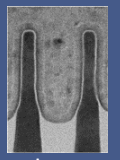


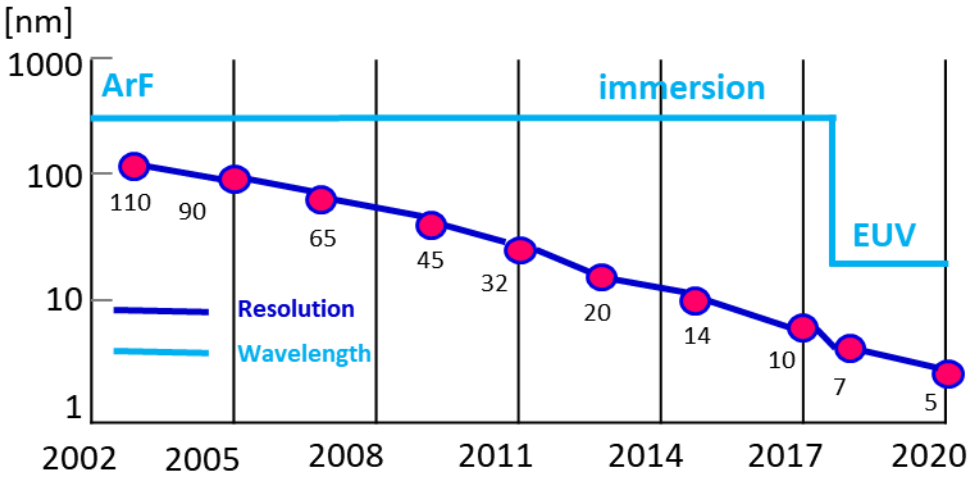
✓ Selective deposition of AlO_x on oxide surface. No AlO_x on W surface

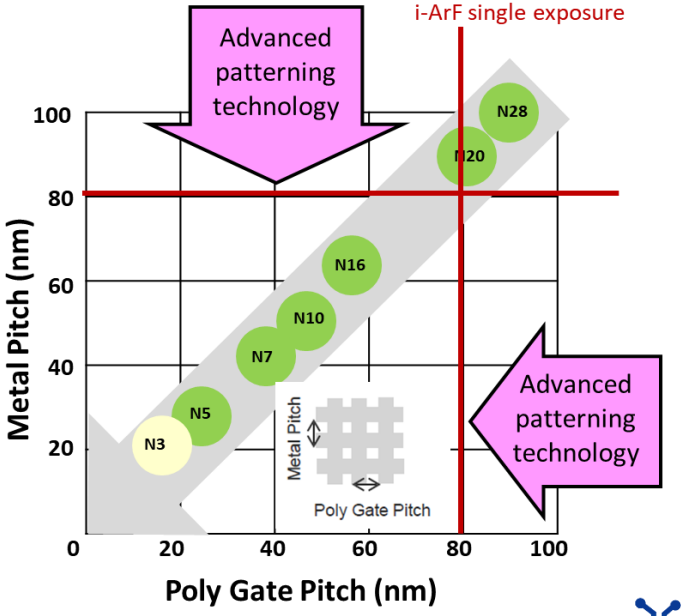
Patterning Technology for Scaling-Down : AS-ALD and Other

Patterning Technology for Scaling-Down

Extreme Ultraviolet (EUV) Lithography

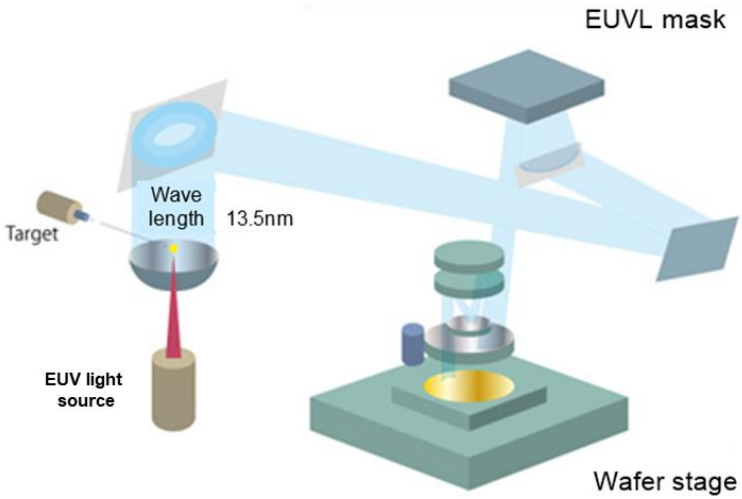
ArF/ArF-i	ArF Immersion + MPT					EUV
90/65nm	45nm	32nm	20nm	14nm	10nm	10nm>
						
Strained Si	ULK	1st Gen HK/MG	1st Gate Last HK/MG	1st Gen FinFET	2nd Gen FinFET	3nd Gen FinFET

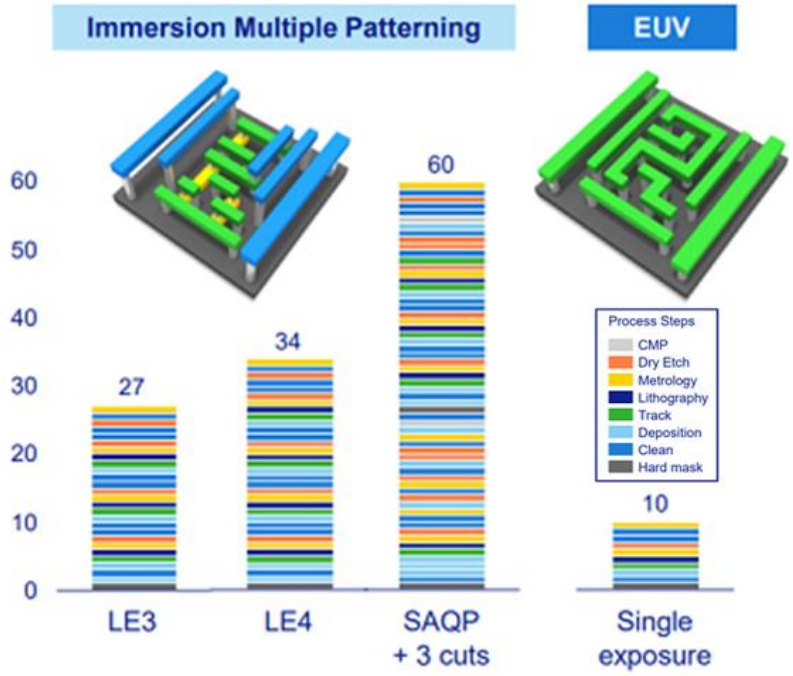




Patterning Technology for Scaling-Down

Extreme Ultraviolet (EUV) Lithography



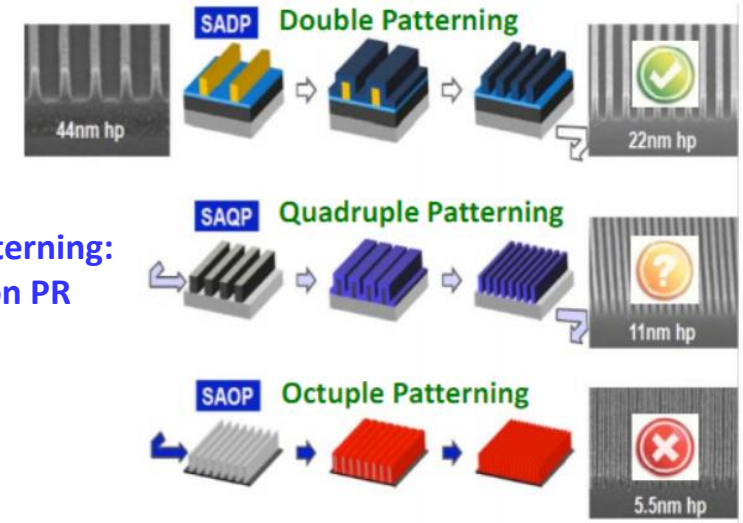


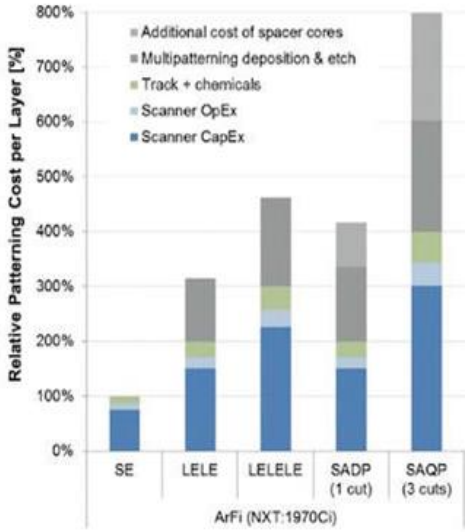
https://www.asml.com/en/products/euv-lithography-systems/twinscan-nxe-3600d

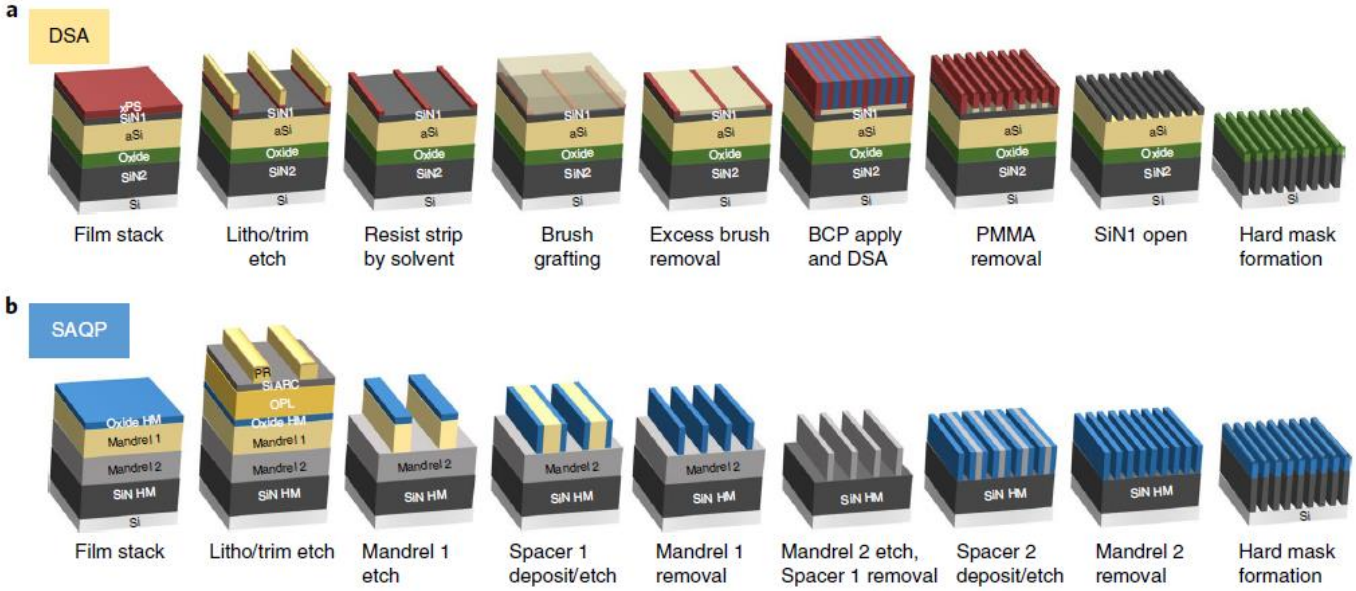
- Considering the number of process and increasing throughput !!
- Introduction for a few nm scale patterning (3-5nm Logic node & Leading DRAM node)

Patterning Technology for Scaling-Down : Cost Issue

Multiple Patterning:
PEALD SiO_2 on PR





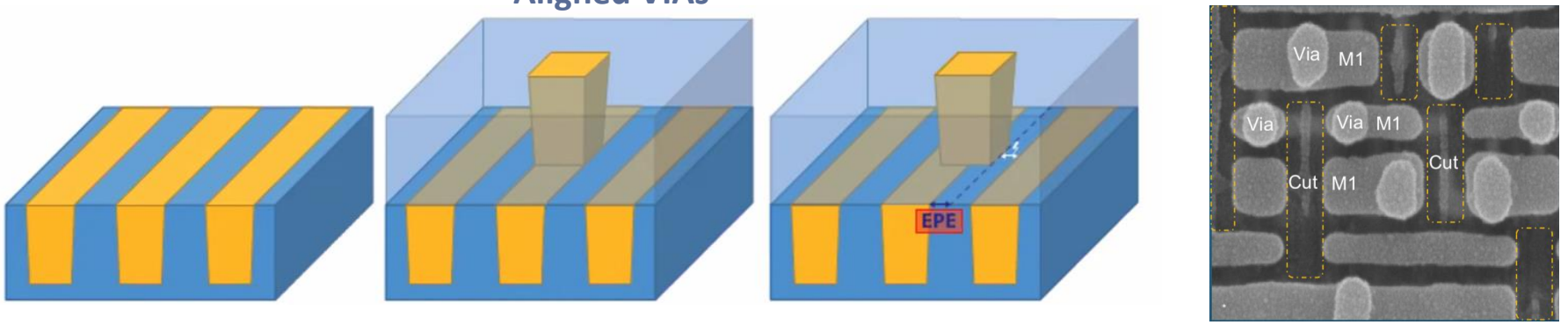


Patterning Technology for Scaling-Down : Top-Down Litho.

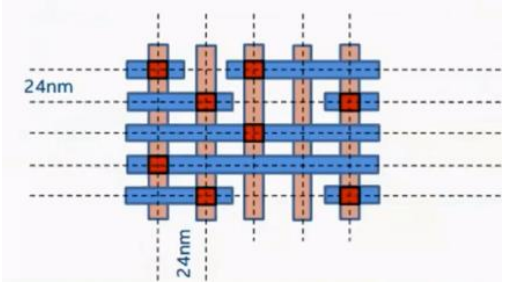
Basic Issues: Self-Aligned VIAs (SAV) with Edge placement error (EPE)

Desired:
Aligned VIAs

In practice:
Edge placement error (EPE)



Small VIAs are difficult to etch → Challenging to fill with metal (Poor yield and performance)



Example) **Twenty trillion chances to fail……**

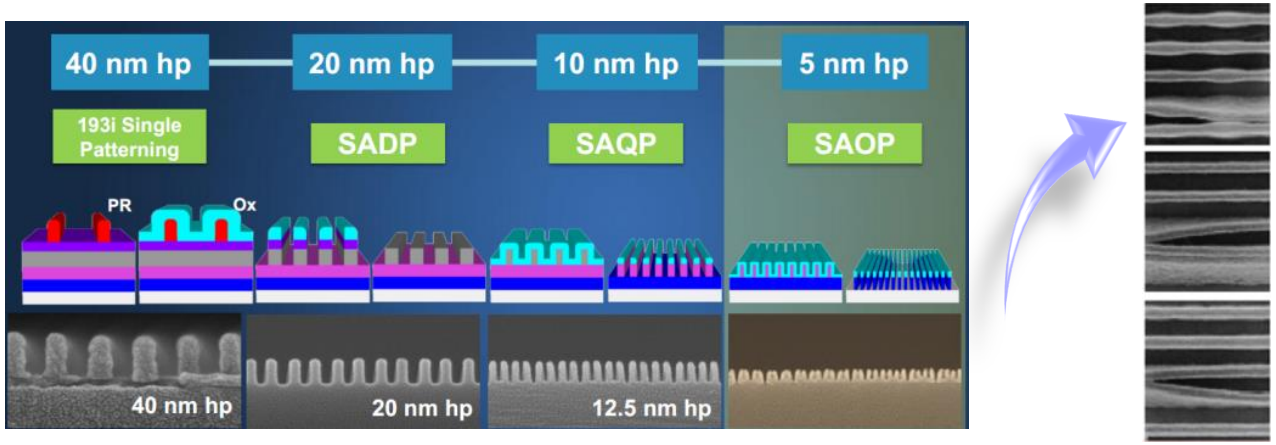
- With a 24 x 24 nm metal pitch grid, there are 123 trillion possible overlap locations on a 300mm wafer.
- If 1 in 6 has a Cut or Via, there are 20 trillion Cuts or Vias on the wafer.
- ~40,000 occurrences of 20 trillion are outside +/-6σ normal distribution.

C. Wallace, 5th Area Selective Deposition Workshop, April 2021

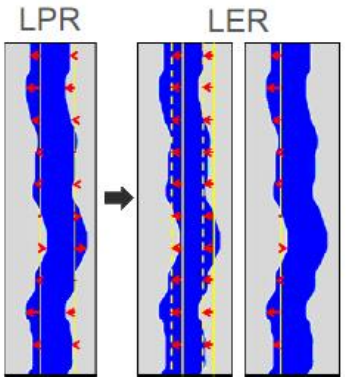
Patterning Technology for Scaling-Down : Top-Down Litho.

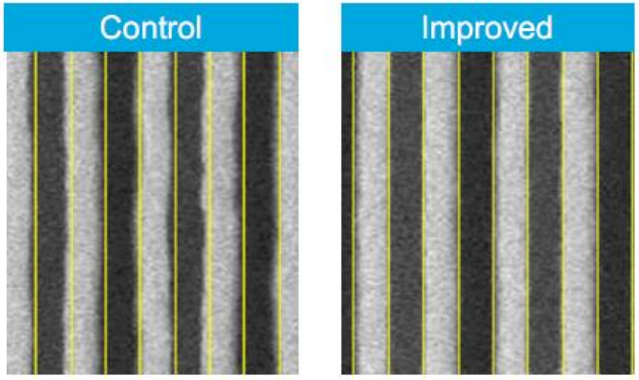
Basic Issues: CD Variation, Roughness, Leaning etc.

■ Critical Dimension → controlling below 10nm

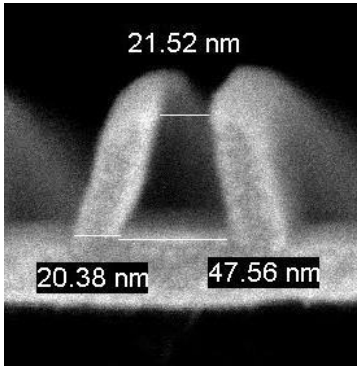


■ Roughness (LER (Line Edge Roughness)/LWR/CER)





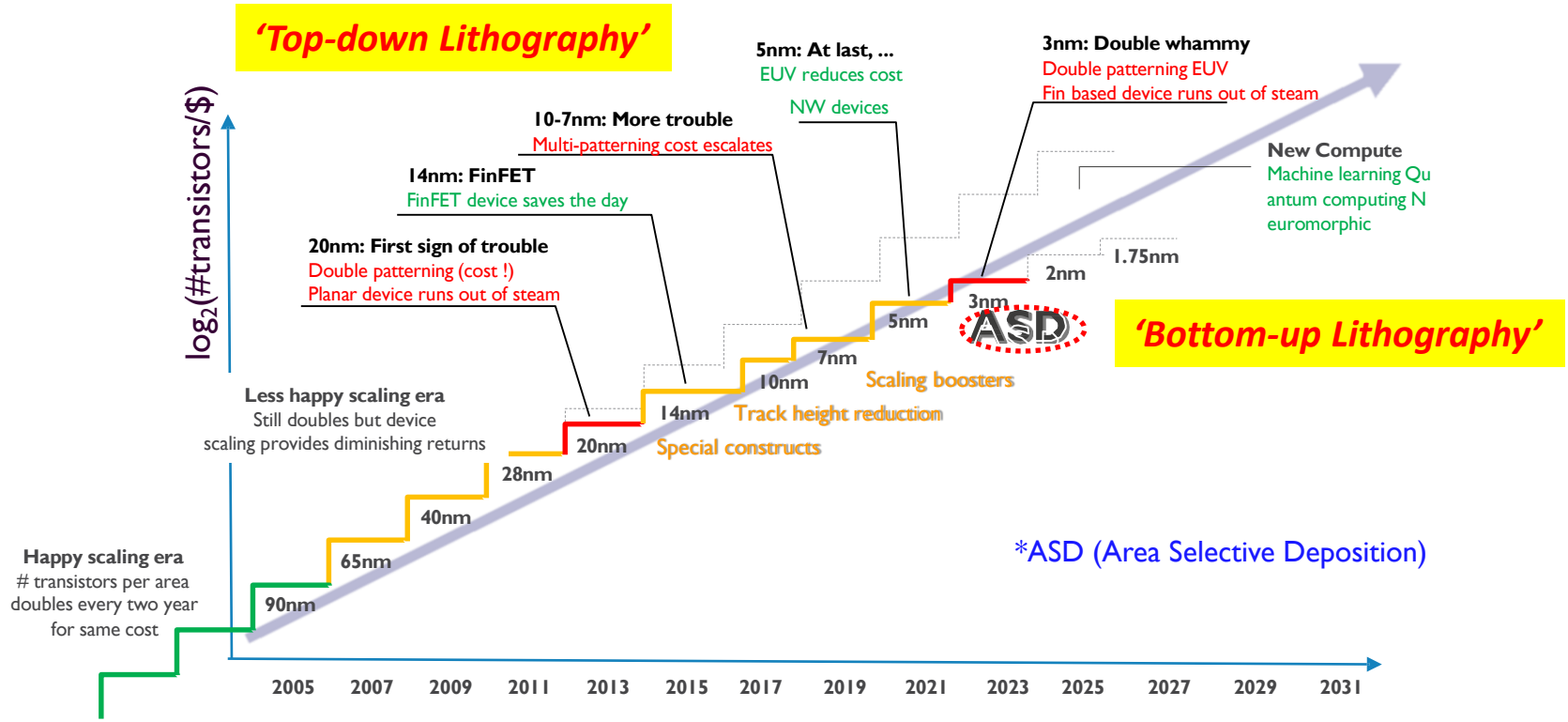
■ Pattern profile (leaning)



Patterning Technology for Scaling-Down

BIG PICTURE - KEEPING MOORE'S LAW

LOGIC SCALING PARADIGM UNDER PRESSURE



Focus of process technology innovation is

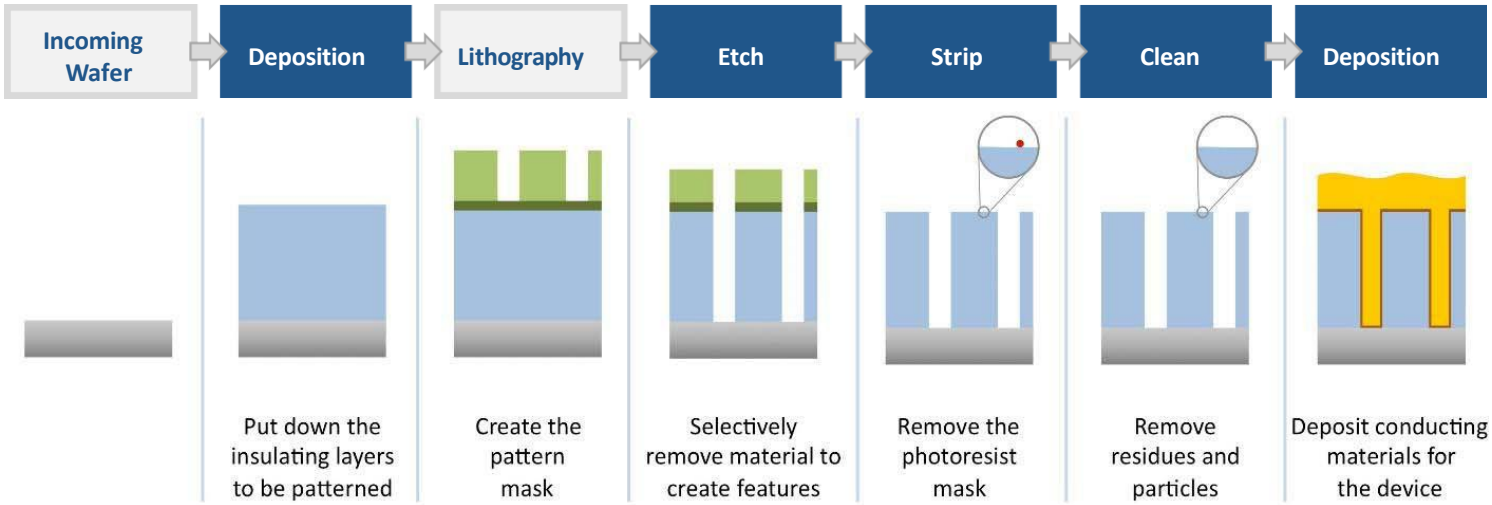
Scale device and wire → Scale basic logic cells → Scale (sub-)system functions

Efrain Altamirano-Sanchez et al., Area Selective Deposition Workshop, April 2019, Leuven

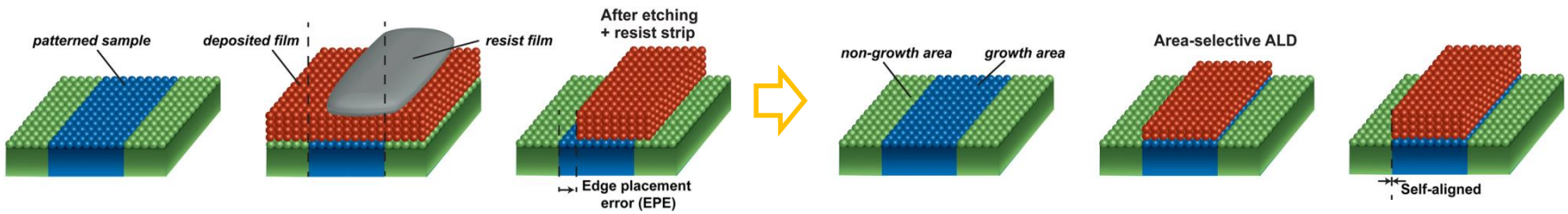
Atomic Layer Processing for Advanced Patterning

■ Conventional wafer fabrication requires many steps across multiple tools

○ **Top-down process**



○ **Bottom-up process**

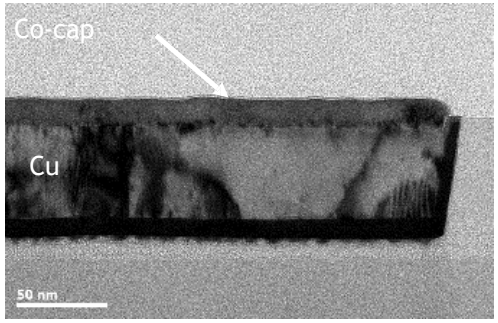


[Lithography & Etch] **[Area Selective Deposition]**

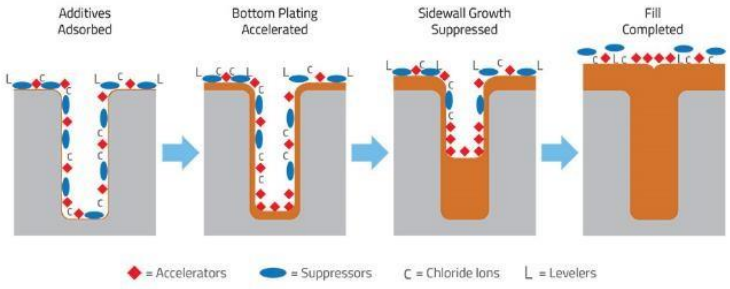
Atomic Layer Processing for Advanced Patterning

■ Current Uses of Selective Deposition in Semiconductor Industry

- Cobalt-capping of Cu lines
  - Metal-on-metal
  - Performed by selective CVD
  - Electro-less cobalt-capping emerging option



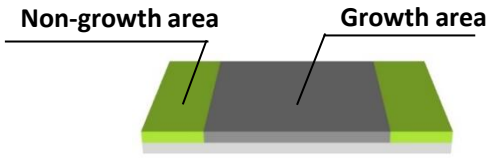
- Bottom-up filling of Cu interconnects
  - Topographically selective
  - Electrochemical bath contains accelerators that preferentially adsorb to the bottom of the feature and suppressors that adsorb to the top



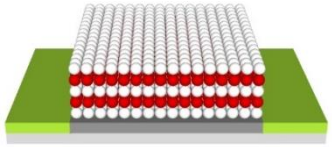
Industry open to selective deposition and more applications need solutions

Atomic Layer Processing for Advanced Patterning

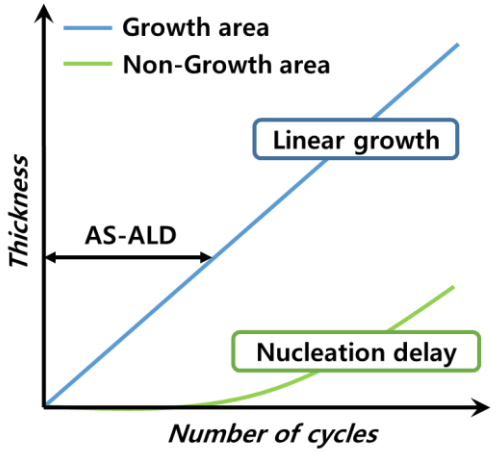
■ Area Selective Atomic Layer Deposition (AS-ALD)



Patterned Surface



After ALD

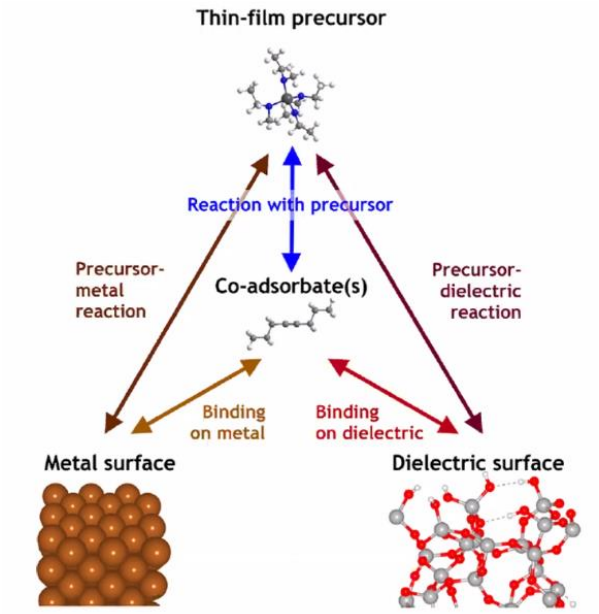


- **Growth to specific areas by exploiting differences in local surface chemistry**
- **Nucleation delay before the growth initiation** on the surfaces that are present **on the same sample**
- **Bottom-up processing** of materials according to **predefined patterns**
- Nanostructure synthesis **without the need for additional process** such as **etching or lift-off**

Atomic Layer Processing for Advanced Patterning

■ Area Selective Atomic Layer Deposition (AS-ALD) : Where is from Selectivity?

Interaction between involved surfaces and molecules

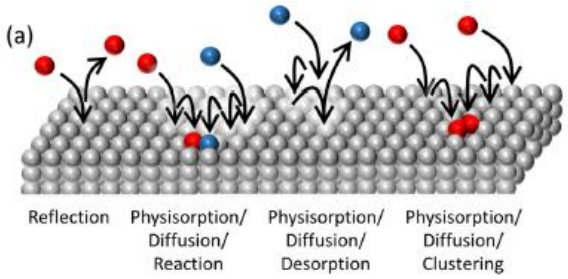


- **Difference in binding of the molecules on the NS and GS**
- **Competitive adsorption!**

* NS : Non-growth surface
* GS : Growth surface

Difference of Reaction energy between GS & NS

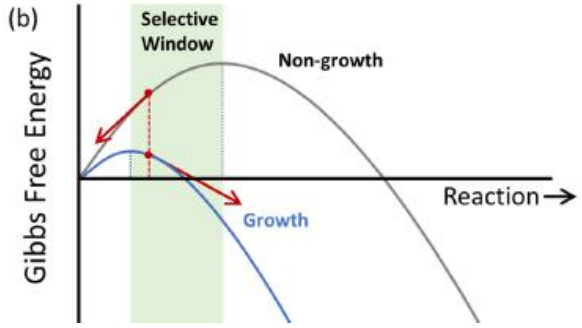
Precursor adsorption & desorption

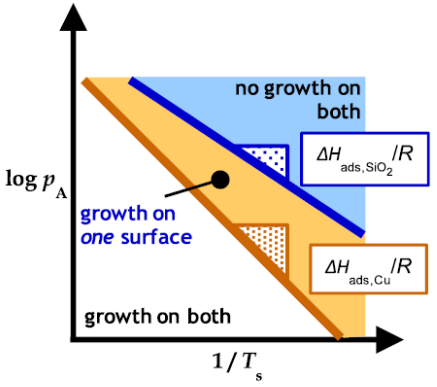


* Stable nuclei on growth surface

* Unstable on the nongrowth surface

➡ **Selective deposition**



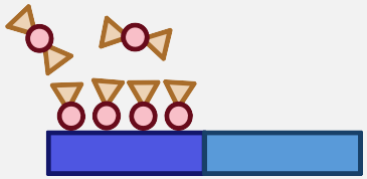


G. Parsons et al., Chem. Mater. 2020 32 4920

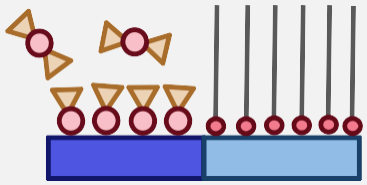
Atomic Layer Processing for Advanced Patterning

■ Strategies for AS-ALD

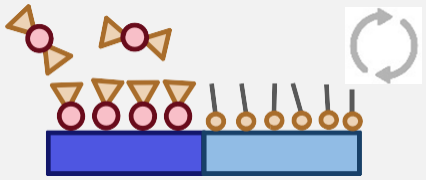
- **Inherent selectivity**



- **Polymer blocking**
  - SAMs



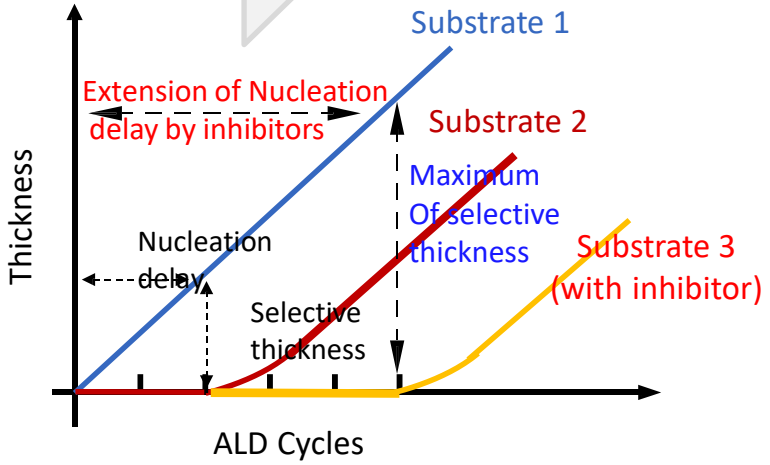
- **Surface inhibition**
  - Small molecules



HVM Requirement for AS-ALD

1. Film Conformality & Property
2. Wafer-to-Wafer Uniformity
3. Defectivity (Particles, Metals)
4. Wafter-to-Wafer Repeatability

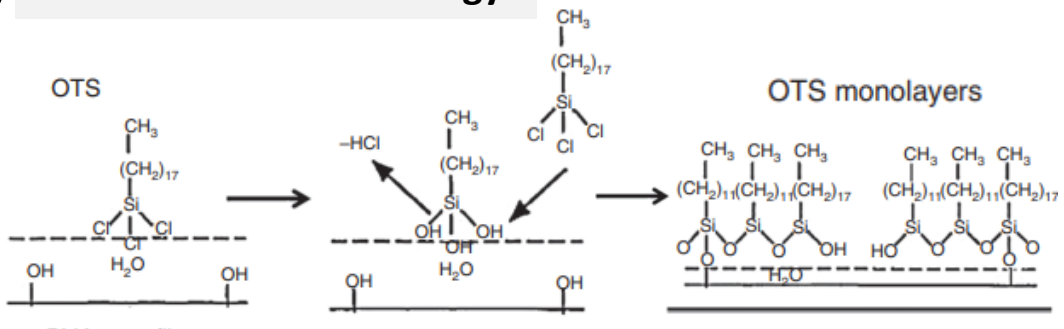
[Nucleation depending on substrates]



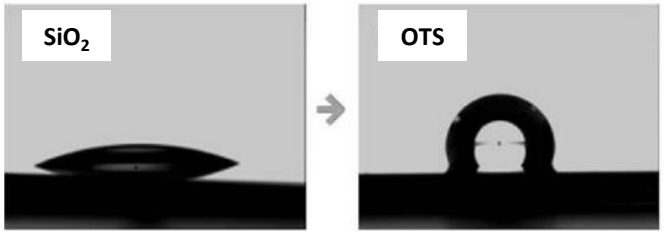
Atomic Layer Processing for Advanced Patterning

SAM – Chemoselective Inhibitor

Control of surface energy

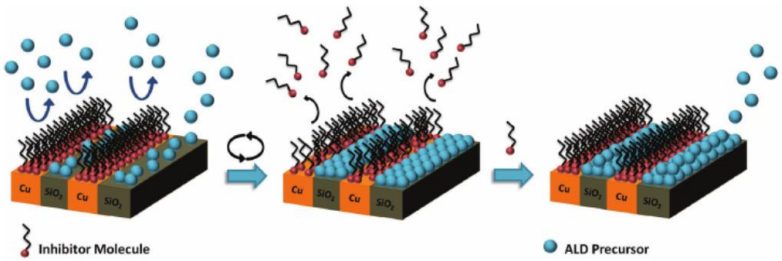


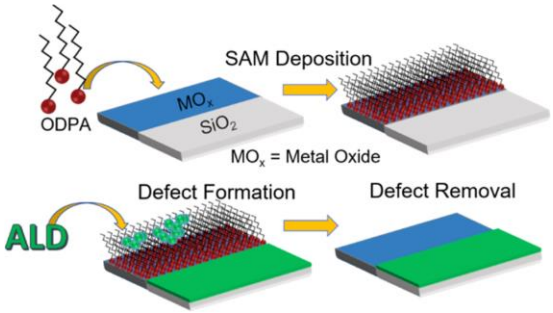
SAM coated Hydrophobic surface

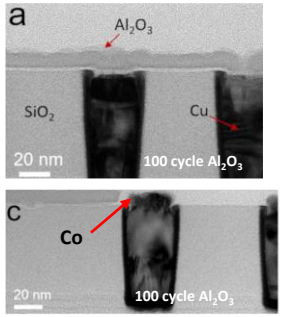


- SAM (Self assembled monolayer) adsorption on silicon oxide surface
- **Hydrophobic functionalization of inhibiting surface**

ASD using SAM in nm-scale







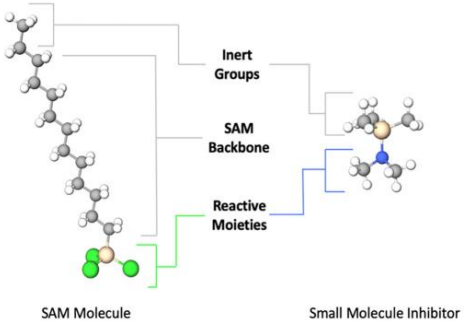
- Selective SAM (Self assembled monolayer) adsorption on metal oxide surface
- **Area selective inhibition (S>90%, ZnO ALD) by** several hundred more cycles of ALD

*ODPA (octadecylephosphonic acid)

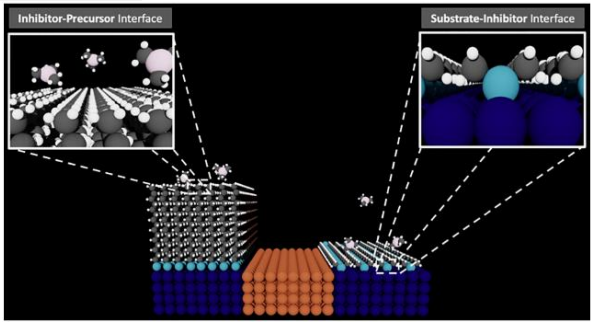
Atomic Layer Processing for Advanced Patterning

SMI – Chemoselective Inhibitor

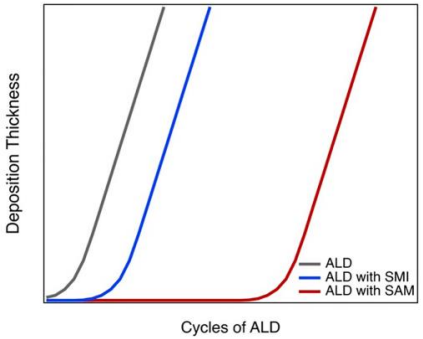
SAM vs SMI (Small molecular Inhibitor)



<Molecular Structure>



<Inhibitors on substrate>



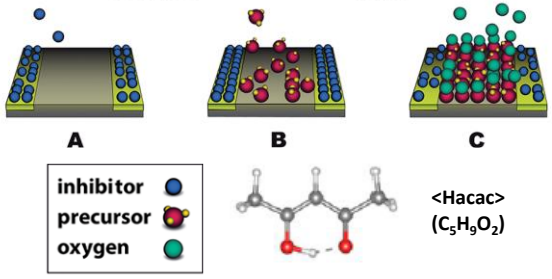
<Inhibiting Property>

- SMI (Small Molecular Inhibitor) : Smaller inert group

  → **Improving Vapor pressure : in-situ Process & Practical Application in Vacuum**

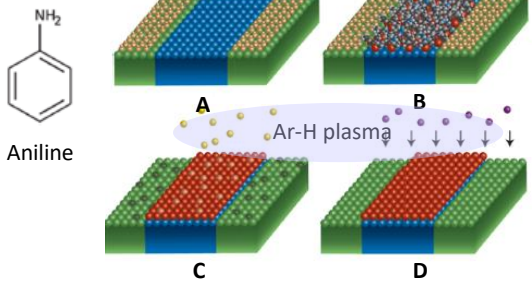
Application of SMI with ALD process

ABC-type SMI recycle

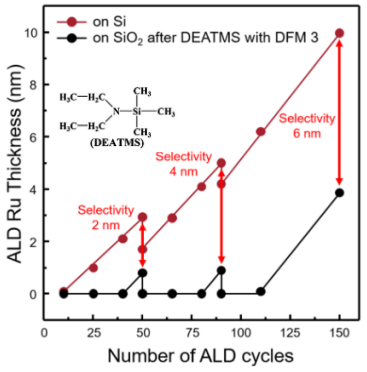


ACS Nano 2017, 11, 9303–9311

ABCD-type SMI recycle



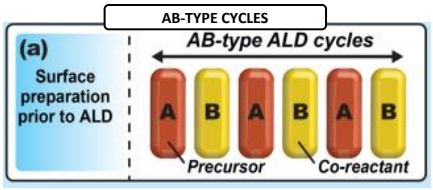
ASD and ALE

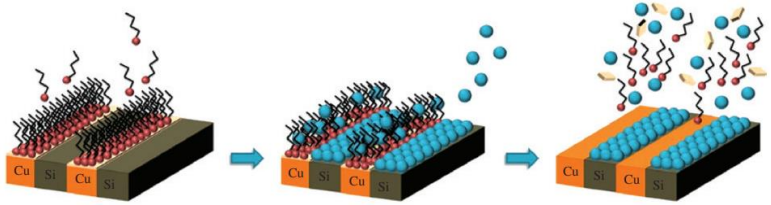


Appl. Surf. Sci. 2021, 539, 148247

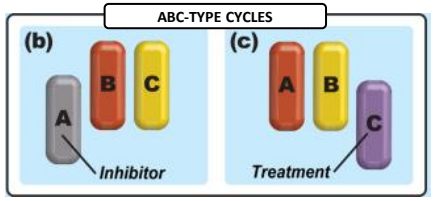
Atomic Layer Processing for Advanced Patterning

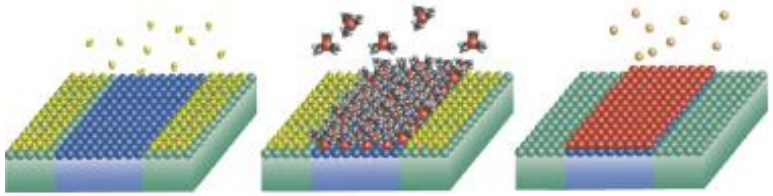
Area selective ALD type



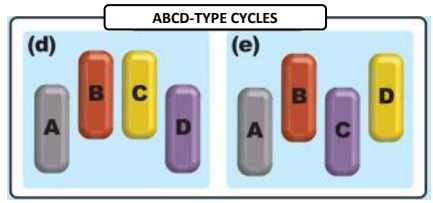


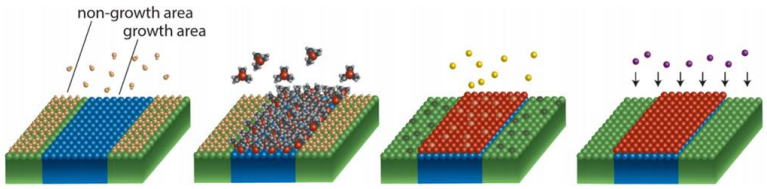
■ Demonstration of SAM patterning through a combination of selective deposition and selective removal of dielectric material.



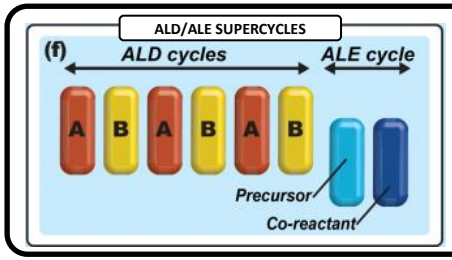


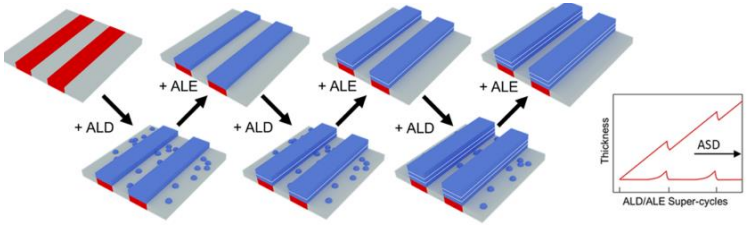
■ ABC-type ALD approach for ASALD using volatile small inhibitor molecules and the precursor ligands are removed by the co-reactant.





■ Demonstration of SAM patterning through a combination of selective deposition and selective removal of dielectric material.



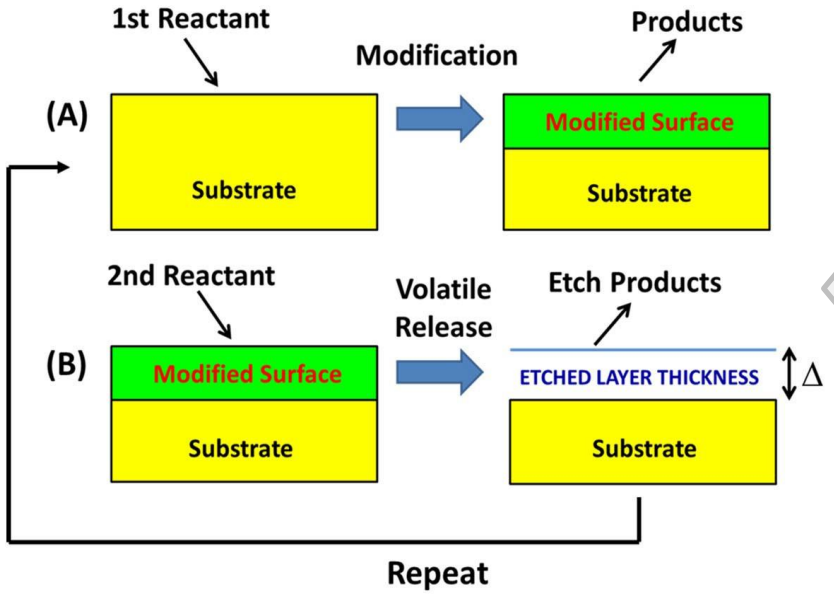


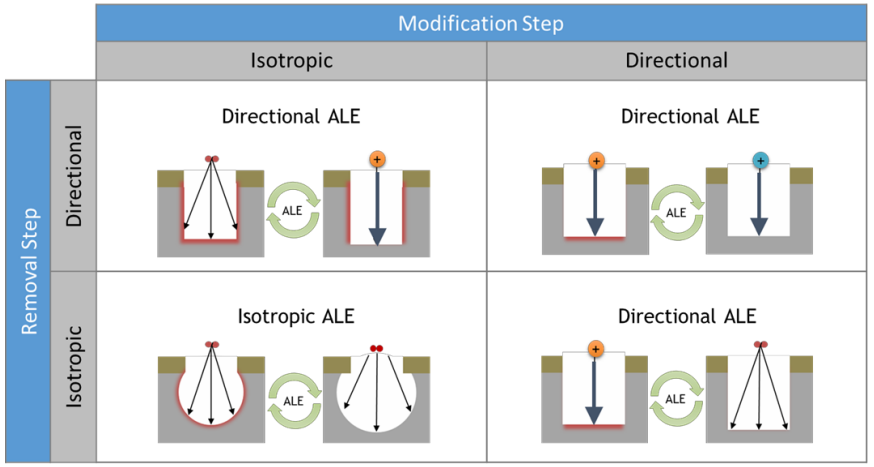
■ Periodic thermal ALE can be successfully integrated into an isothermal ALD/ALE supercycle scheme

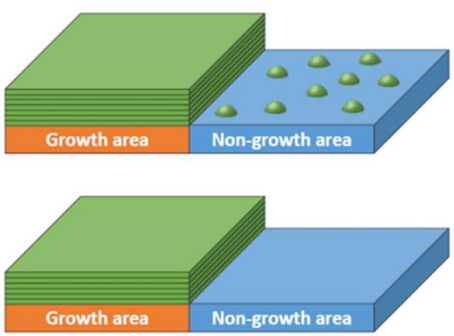
Nanotechnol Rev 2017; 6(6): 527–547
Chem. Mater. 2019, 31, 4793−4804
Chem. Mater. 2019, 31, 2−12
Chem. Mater. 2020, 32, 3335−3345

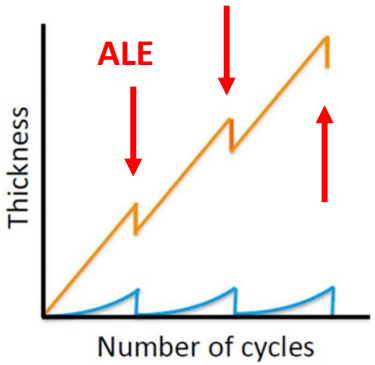
Atomic Layer Processing for Advanced Patterning

Atomic Layer Etching (ALE)







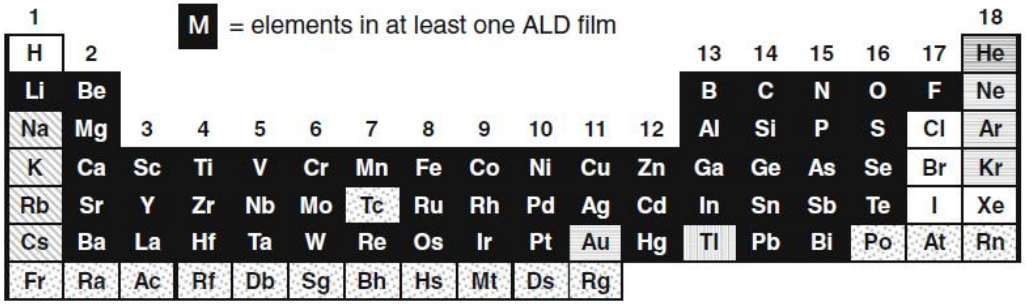


- Starting point: deposition occurs at a faster rate on the growth area
- ALE is performed to remove any deposited atoms From the non-growth area
- Supercycle is repeated until the desired thickness is reached

Metal ALD
: Ru & transition metal

Atomic Layer Deposition for Pure Metal

- **ALD Precursors and the associated materials on the Periodic Table**



Oxide dielectrics	Al_2O_3, TiO_2, ZrO_2, HfO_2, Ta_2O_5, Nb_2O_5, Sc_2O_3, Y_2O_3, BeO, MgO, B_2O_3, SiO_2, GeO_2, La_2O_3, CeO_2, PrO_x, Nd_2O_3, Sm_2O_3, EuO_x, Gd_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, Yb_2O_3, Lu_2O_3, $SrTiO_3$, $BaTiO_3$, $PbTiO_3$, $PbZrO_3$, Bi_xTi_yO, Bi_xSi_yO, $SrTa_2O_6$, $SrBi_2Ta_2O_9$, $YScO_3$, $LaAlO_3$, $NdAlO_3$, $GdScO_3$, $LaScO_3$, $LaLuO_3$, $LaYbO_3$, $Er_3Ga_5O_{13}$
Oxide conductors or semiconductors	In_2O_3, In_2O_3:Sn, In_2O_3:F, In_2O_3:Zr, SnO_2, SnO_2:Sb, SnO_2:Al, SnO_2:N, Sb_2O_3, ZnO, ZnO:Al, ZnO:B, ZnO:Ga, RuO_2, RhO_2, IrO_2, Ga_2O_3, VO_2, V_2O_5, WO_3, W_2O_3, NiO, CuO_x, FeO_x, CrO_x, CoO_x, MnO_x
Other ternary oxides	$LaCoO_3$, $LaNiO_3$, $LaMnO_3$, $La_{1-x}Ca_xMnO_3$
Nitride dielectrics or semiconductors	BN, AlN, GaN, InN, Si_3N_4, Ta_3N_5, Cu_3N, Zr_3N_4, Hf_3N_4, LaN, LuN
Metallic nitrides	TiN, Ti-Si-N, Ti-Al-N, TaN, NbN, MoN, WN_x, WN_xC_y, Co_xN, Sn_xN
II-VI semiconductors	ZnS, ZnSe, ZnTe, CaS, SrS, BaS, CdS, CdTe, MnTe, HgTe
II-VI based phosphors	ZnS:M (M=Mn,Tb,Tm); CaS:M (M=Eu, Ce, Tb, Pb); SrS:M(M=Ce,Tb, Pb)
III-V semiconductors	GaAs, AlAs, AlP, InP, GaP, InAs
Fluorides	CaF_2, SrF_2, MgF_2, LaF_3, ZnF_2
Elements	Ru, Pt, Ir, Pd, Rh, Ag, Cu, Ni, Co, Fe, Mn, Ta, W, Mo, Ti, Al, Si, Ge, Sb
Other semiconductors	PbS, SnS, In_2S_3, Sb_2S_3, Cu_xS, $CuGaS_2$, WS_2, SiC, $Ge_2Sb_2Te_5$
Others	La_2S_3, Y_2O_2S, TiC_x, TiS_2, TaC_x, WC_x, $Ca_3(PO_4)_2$, $CaCO_3$, organics

ALD Difficulties:

- Oxide
- Nitride
- Sulfide
- Element/Carbide

Harder

Because of Chemistry
: Precursor & Reaction

Atomic Layer Deposition for Pure Metal

Requirement for metal ALD

❑ Requirements of Metal ALDs

1. Nucleating well on a certain surface.
2. Providing films with the smallest possible surface roughness.
3. Giving continuous films even at thicknesses of a few nanometers.
4. Depositing the film as low deposition temp. (<150^{o}C) as possible.
5. Low impurities in the films

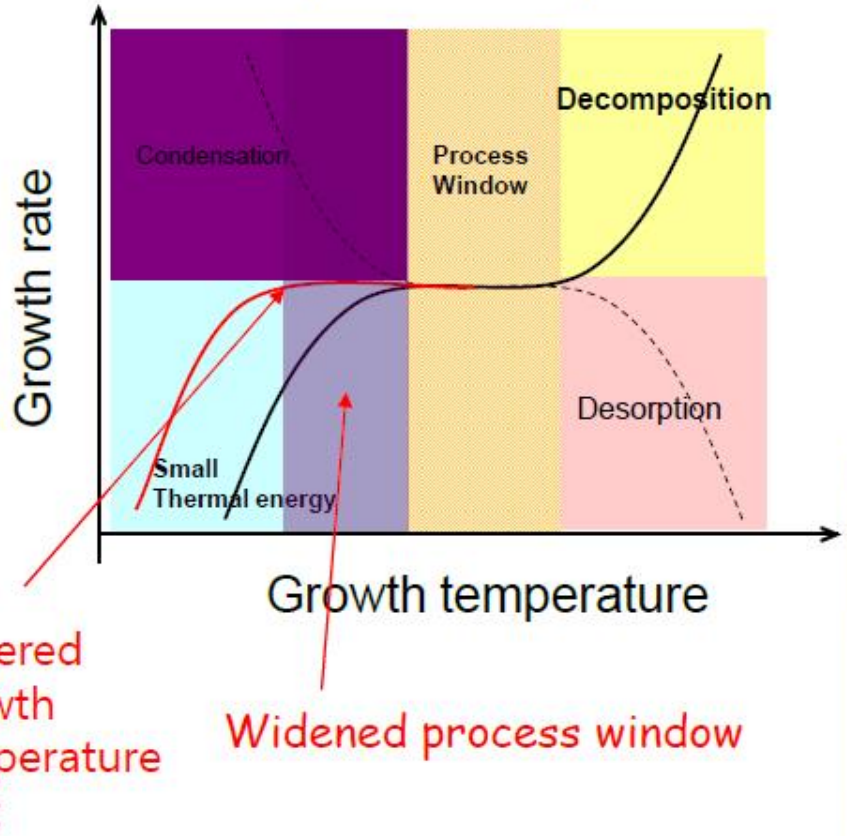
⇨ Unfortunately, **low temperatures** limit surface mobility and minimize the tendency of the metal atoms to form islands at low thicknesses and rough films at higher thicknesses !!

⇨
1. Suitable Precursors for metal ALDs
2. Highly reactive reagents as a reactant
3. Novel chemical routes for metal chemical reactions.

Atomic Layer Deposition for Pure Metal

♦ **Higher reactivity of radicals**

- **Large "process window"**
- **Low temperature deposition**



- **More versatile reactions**

Metal precursor + H N O

→ Metals Nitrides Oxides

Atomic Layer Deposition for Pure Metal

Electrochemical Potentials

❑ Metallic first row transition

$M^{2+} + 2e^- \leftrightarrow M$	E° (V)
Cu	0.3419
Ni	−0.257
Co	−0.280
Fe	−0.447
Mn	−1.185
Cr	−0.913
V	−1.175
Ti	−1.630

☞ Reactivity of metal precursor with common reducing agents ↓

↔ ALD growth on temperature ↑

☞ Cu (II) has a positive E^o value : Possible Metal ALD!

☞ Ni(II), Ti(III)… have negative E^o values : Challengeable Metal ALD!

Thermal ALD growth of is only well developed for noble metals, Mo, W, and Sb, Due in large part to their more positive E^o values.

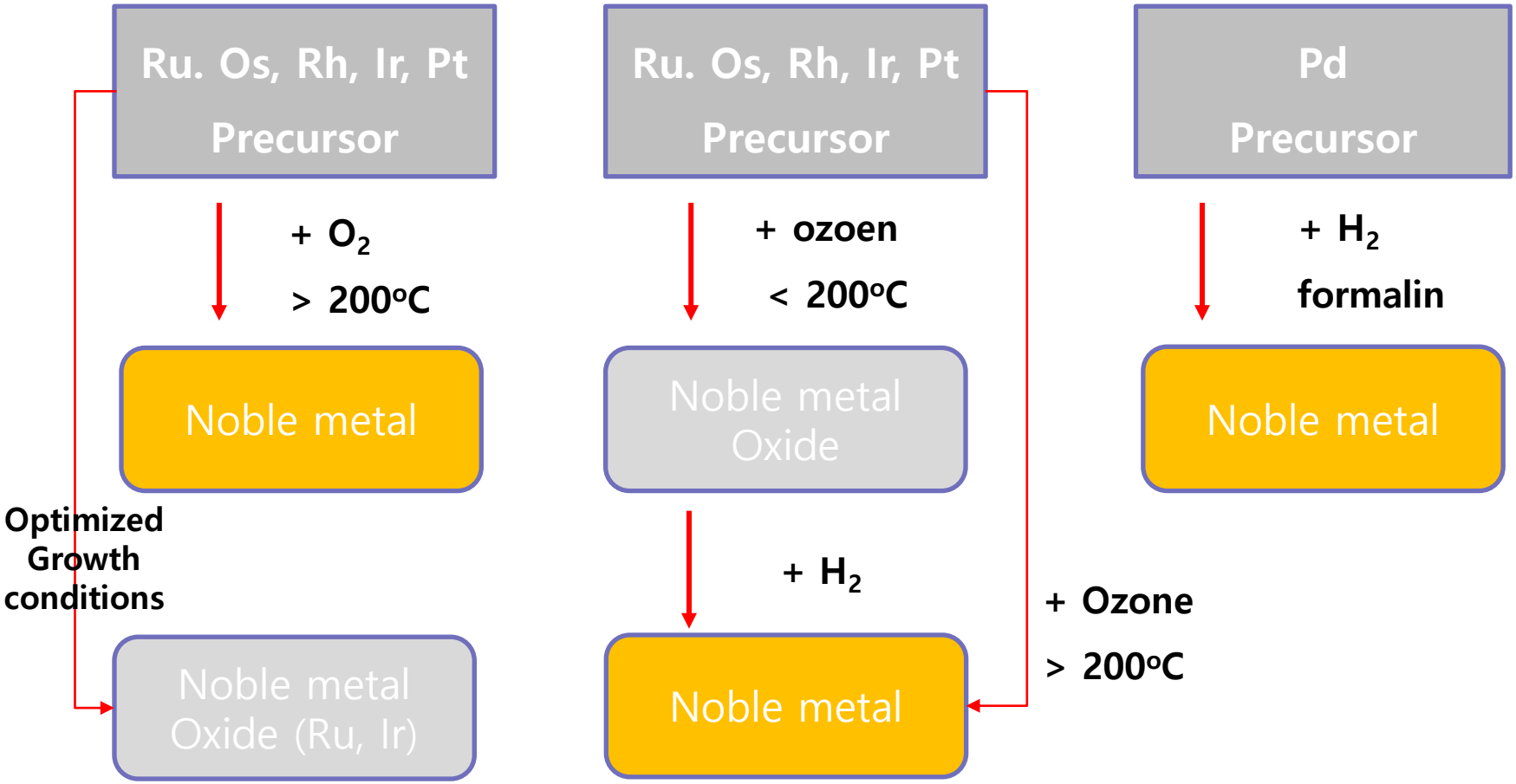
Atomic Layer Deposition for Pure Metal

- **The type of Co-reactant for metal ALD (based on peer review papers)**

1. O_2 (including air) and O_3
2. H_2
3. O_2, O_3 or H_2O followed by H_2
4. Main group hydrides (hydrosilanes, hydroboranes and hydroalanes)
5. Amines and hydrazines
6. CxHyOz organic molecules (formaldehyde, glyoxylic acid, formic acid, and alcohols)
7. Zn metal
8. $ZnEt_2$
9. $AlMe_3$

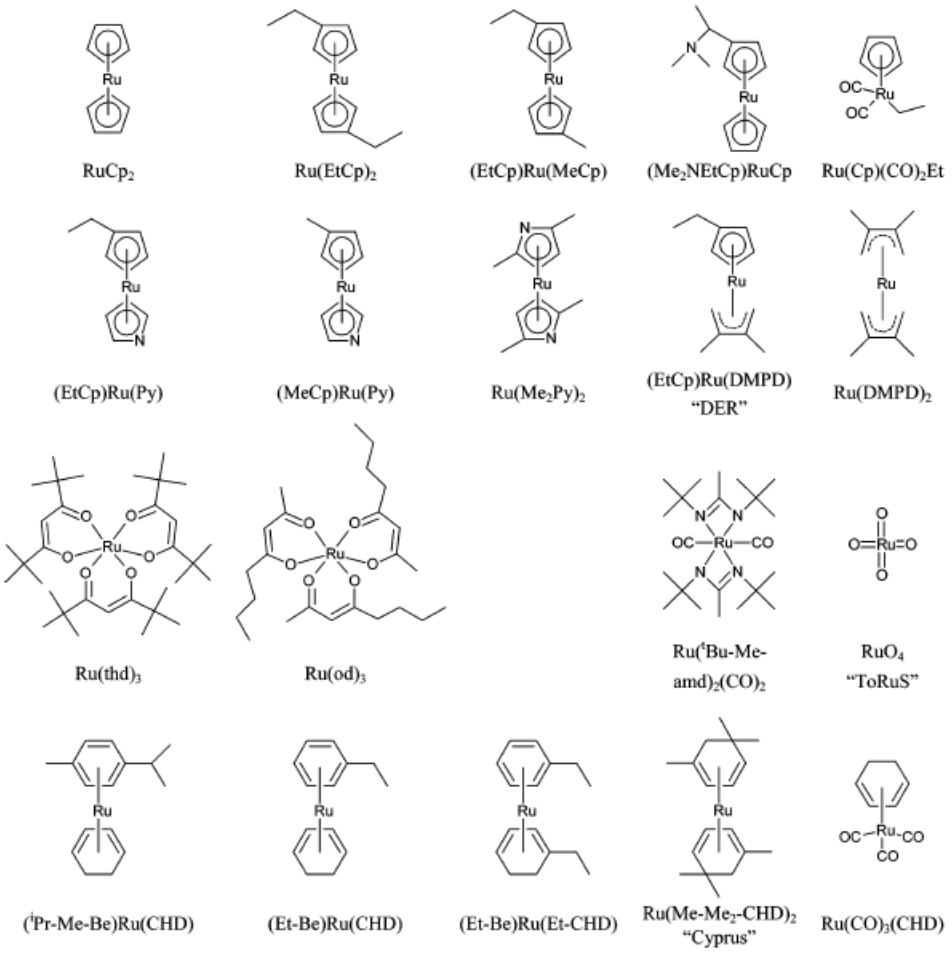
Atomic Layer Deposition for Noble Metal

- **Simplified flowchart for noble metals and their oxides**



Atomic Layer Deposition for Ru Metal

- **Ruthenium precursors reported for Ru ALD Processes**



Atomic Layer Deposition for Ru Metal

metal precursor	T_{vap} (°C)	reactant	T_{dep} (°C)	growth rate (Å cycle^{-1})
$RuCp_2$	50	O_2 (air)	275–400	$0.1^{275\ °C}$, $0.3^{300\ °C}$, $0.4^{325\ –375\ °C}$, $0.5^{400\ °C}$
	60	O_2	225–275	$0.1^{225\ °C}$, $0.3^{250\ °C}$, $0.4^{275\ °C}$
	80	O_2	245	0.2–0.3
		O_2 (air)	250	0.2
		O_2	270	0.5
	50	O_2	275	1
	80	O_2	310–350	1
	85	O_2	300, 350	$1.2^{300\ °C}$
$Ru(EtCp)_2$	80	O_2	270	0.7, 1.5
	80	O_2	270	1.0
		O_2	300	0.4
	80	O_2	300	0.5
	65	O_2	300	1.8
$Ru(EtCp)_2$		ozone	225–275	$0.9^{225\ °C}$, $1.1^{250\ °C}$, $1.2^{275\ °C}$
(EtCp)Ru(MeCp)	45	O_2	250–325	$0.2–0.3^{250\ °C}$, $0.4–0.5^{275–300\ °C}$
$(Me_2NEtCp)RuCp$	75–80	O_2 (air)	325–500	$0.2^{325–350\ °C}$, $0.4^{375\ °C}$, $0.5^{400–450\ °C}$, $0.8^{500\ °C}$
(EtCp)Ru(DMPD)		O_2	250	0.4
(EtCp)Ru(DMPD) in ECH		O_2	210–290	$0.2^{210\ °C}$, $0.3–0.4^{230\ °C}$, $0.4–0.5^{250\ °C}$, $0.3–0.5^{290\ °C}$
	200	O_2	230–280	$0.4^{225\ –250\ °C}$, $0.5^{280\ °C}$
		O_2	250	0.3
	230	O_2	280	0.5
$Ru(DMPD)_2$	60	O_2	175–250	$<0.1^{175–210\ °C}$, $0.1^{225–250\ °C}$
	82	O_2	325	0.6
(EtCp)Ru(Py)	55	O_2	275–350	$0.3–0.5^{275\ °C}$, $0.2–0.4^{300\ °C}$, $0.4–0.6^{325\ °C}$, $0.5–0.6^{350\ °C}$
(MeCp)Ru(Py)		O_2	NA	0.4–0.6
$Ru(Me_2Py)_2$	55–60	O_2	250–325	$0.2^{250\ °C}$, $0.6^{300\ °C}$
$Ru(Cp)(CO)_2Et$	85	O_2	200–325	$0.8–0.9^{300\ °C}$
	90	O_2	325	1.0
$Ru(thd)_3$	100	O_2 (air)	325–450	$0.3^{325\ °C}$, $0.4^{350–400\ °C}$, $0.5^{450\ °C}$
	100	O_2	250, 325	$0.2^{250\ °C}$, $0.4^{325\ °C}$
$Ru(thd)_3$ in ECH		O_2	330, 380	$0.3^{380\ °C}$
$Ru(od)_3$ in *n*-butylacetate	200	O_2	275–450	$0.6^{275–300\ °C}$, $0.8^{325–375\ °C}$, $1.0^{400\ °C}$, $1.8^{425\ °C}$, $2.0^{450\ °C}$
(^{i}Pr-Me-Be)Ru(CHD)	120	O_2	185–310	$0.6^{185\ °C}$, $0.8^{200\ °C}$, $0.9^{225–270\ °C}$, $1.3^{310\ °C}$
	100	O_2	220	0.9–1.0
	120	O_2	225	0.8
	100	O_2	140–350	0.9^{NA}
(Et-Be)Ru(CHD)	100	O_2	140–350	0.9^{NA}
(Et-Be)Ru(Et-CHD)	100	O_2	140–350	$0.4^{225\ °C}$
$Ru(Me\text{-}Me_2\text{-}CHD)_2$	60	O_2	200–325	$0.1^{200\ °C}$, $0.3^{235\ °C}$, $0.5^{250–310\ °C}$, $0.2^{325\ °C}$
	60	O_2	NA	0.5
$Ru(CO)_3(CHD)$		NH_3	200	3.5–4
$Ru(^tBu\text{-}Me\text{-}amd)_2(CO)_2$	140	O_2	300–400	$0.5^{300\ °C}$, $1.0^{325\ °C}$, $1.5^{350\ °C}$, $1.7^{400\ °C}$
$Ru(^tBu\text{-}Me\text{-}amd)_2(CO)_2$	130	NH_3	200–300	$0.08^{250\ °C;\ 0.06\ CVD}$, $0.3^{280\ °C;\ 0.15\ CVD}$, $0.7^{300\ °C;\ 0.4\ CVD}$
ToRuS	RT	H_2	100–200	$1.3^{100–175\ °C}$, $1.4^{200–225\ °C}$, $1.5^{250\ °C}$
	25	H_2	>150, >200	1.8^{NA}

[a]Abbreviations: NA, not available; RT, room temperature.

❑ Reactants

Most Ligand: Cp

1. **Oxygen or Air**
2. Ozone
3. NH3
4. H2

Atomic Layer Deposition for Ru Metal

Table 3. Impurity Contents of Ru ALD Processes

cycle sequence	T_{dep} (°C)	impurity contents (atom %)	method
$Ru(Cp)_2-O_2$ (air)	300	O <1.5, C <0.3, H <0.4	TOF-ERDA
	350	O <0.4, C <0.2, H <0.2	TOF-ERDA
	400	O <0.5, C <0.3, H <0.2	TOF-ERDA
$Ru(Cp)_2-O_2$	245	O in surface and in film	AES
$Ru(EtCp)_2-O_2$	270	O <2, C <2	TOF-ERDA, AES
$Ru(EtCp)_2$–ozone	275	O <1	AES
(EtCp)Ru(DMPD) in ECH–O_2	250, 280	O <AES limit	AES
	280	negligible O and C	XPS
$Ru(DMPD)_2-O_2$	325	O <1, C <0.2, N < 0.2	SIMS
(EtCp)Ru(Py)–O_2	275	O <2, C 0.6, H 2, N 0.5	TOF-ERDA
(MeCp)Ru(Py)–O_2	NA	O 10, C <1.3, H <2	ERDA
$Ru(Me_2Py)_2-O_2$	275	O 3.6, C 1.6, H 3, N 1.2	TOF-ERDA
$Ru(thd)_3-O_2$ (air)	350	O 4.1, C 1.2, H 2.2	TOF-ERDA
$Ru(thd)_3$ in ECH–O_2	380	O <1	SIMS
(^{i}Pr-Me-Be)Ru(CHD)–O_2	220	O ~4	XPS
	225	O <SIMS limit, C ~1.8	SIMS
	270	O <SIMS limit, C <SIMS limit	SIMS
	310	O <SIMS limit, C ~2.4	SIMS
$Ru(^tBu\text{-}Me\text{-}amd)_2(CO)_2-O_2$	NA	O 0.3, C 0.3	APM
$Ru(^tBu\text{-}Me\text{-}amd)_2(CO)_2-NH_3$	300	O ~0.2%, C ~0.05%	SIMS
	NA	O, C, N < RBS limit	RBS
ToRuS–H_2	100, 200	O 3, C 0.5–1, H <1, N < 1	ERDA
	250	O <AES limit, C <AES limit	AES

- ❑ Very low impurities in the films
- ❑ High Deposition Temperature (>250°C)

Atomic Layer Deposition for Transition Metal

Dihydrogen

- Only undergo ALD with H_2 at high temperature (250-400°C)
- AMD classes as ligands may react with H2 on relatively low temperature.
  : via a result of amidinate anion hydrogenation

Table 2
Metal precursor/co-reactant combinations that have been used for metal ALD or pulsed-CVD and employ H_2 as the co-reactant (not in combination with O_2, O_3 or H_2O). This table focuses on initial literature reports for each metal precursor/co-reactant combination. The first column of the table indicates whether ALD or pulsed-CVD is claimed, although in a number of cases in Tables 1–7 ALD is claimed without demonstration of self-limiting growth.

Deposited metal (ALD or CVD)	Substrate	Metal precursor	Co-reactant	Reaction temp. (°C)	Year	Reference
Mn (CVD)	Various	$Mn(amd^{iPr,nBu})_2$	H_2	300	2010	Gordon et al. [76]
Fe (ALD)	Si, C, glass, WN	$Fe_2(amd^{tBu})_2$	H_2	250	2003	Gordon et al. [77,78]
Ru (CVD)	SiO_2 or Al_2O_3	$Ru(thd)_3$	H_2	140	2003	Lashdaf et al. [79]
Ru (ALD)	SiO_2	$Ru(acac)_3$	H_2	300–370	2007	Gelfond et al. [80]
Co (ALD)	Si, C, glass, WN	$Co_2(amd^{iPr})_2$	H_2	260–350	2003	Gordon et al. [77,78]
Rh (CVD)	SiO_2	$\{RhCl(CO)_2\}_2$	H_2	75–100	1995	Kalck et al. [81,82]
Rh (CVD)	SiO_2	$Rh(allyl)_3$	H_2	60–80	1995	Kalck et al. [81,82]
Rh (CVD)	SiO_2	$(acac)Rh(CO)_2$	H_2	85–100	1995	Kalck et al. [81,82]
Ir (ALD)	SiO_2	IrF_6	H_2	375	2005	Dussarrat et al. [83]
Ni (ALD)	Ti or Al	$Ni(acac)_2$	H_2	250	2000	Niinistö et al. [84]
Ni (ALD)	Si, C, glass, WN	$Ni_2(amd^{iPr})_2$	H_2	250	2003	Gordon et al. [77,78]
Pd (ALD)	Ir or Pd	$Pd(hfac)_2$	H_2	80	2003	Senkevich et al. [85]
Pd (CVD)	SiO_2 or Al_2O_3	$Pd(thd)_2$	H_2	90	2003	Lashdaf et al. [79]
Pd (ALD)	Air oxidized Ta	$Pd(hfac)_2$	H_2	80	2006	Lu et al. [86]
Pd (CVD)	Glass or silica powder	$(hfac)Pd(allyl)$	H_2	45–60	1996	Kalck et al. [82,87,88]
Pd (CVD)	Glass or silica powder	$CpPd(allyl)$	H_2	30–60	1996	Kalck et al. [82,87,88]
Pt (CVD)	Glass or silica powder	$PtMe_2(COD)$	H_2	90	2000	Kalck et al. [81,88]
Pt (CVD)	Ti, Al, SiO_2	$Pt(acac)_2$	H_2	250	2000	Niinistö et al. [84]
Cu (ALD)	Ta	CuCl	H_2	360–410	1997	Mårtensson et al. [89]
Cu (ALD)	Pd/Pt, TiN, ITO, Ta, Fe or Ni	$Cu(thd)_2$	H_2	190–260	1998	Mårtensson et al. [18]
Cu (nd)[a]	Ti or Al	$Cu(acac)_2$	H_2	250	2000	Niinistö et al. [84]
Cu (ALD)	Si, C, glass, or Co on WN	$Cu_2(amd^{iPr})_2$	H_2	280	2003	Gordon et al. [77,78]
Cu (ALD)	SiO_2, Si_3N_4, Co, WN	$Cu_2(amd^{sBu})_2$	H_2	150–190	2005	Gordon et al. [75,90]
Cu (nd)[a]	TiN	$Cu(hfac)_2$	H_2, pyridine	25–100	2010	Chang et al. [91]

[a] nd = not determined.

D. Emslie et al. J. Coor. Chem. Rev. 257 (2013)

Atomic Layer Deposition for Transition Metal

- **Dioxygen, ozone or water, followed by dihydrogen**

  - Two-Step ALD : Oxidation and then the followed by dihydrogen (reducing)
    : Two separate non-alternating steps (PEALD cases)
    : The metal film may be unexpected in terms of physical/chemical/electrical prop.

Metal precursor/co-reactant combinations that have been used for metal ALD or pulsed-CVD and employ both (a) O_2, O_3 or H_2O, and (b) H_2 as co-reactants. This table focuses on initial literature reports for each metal precursor/co-reactant combination. The first column of the table indicates whether ALD or pulsed-CVD is claimed, although in a number of cases in Tables 1–7 ALD is claimed without demonstration of self-limiting growth.

Deposited metal (ALD or CVD)	Substrate	Metal precursor	Co-reactant	Reaction temp. (°C)	Year	Reference
Ir (ALD)	SiO_2, Al_2O_3 or glass	$Ir(acac)_3$	O_3, then H_2	165–200	2009	Hämäläinen et al. [92]
Ir (ALD)	Al_2O_3	Cp'Ir(CHD)	O_3, then H_2	120–180	2011	Hämäläinen et al. [93]
Cu (ALD)	Al_2O_3, SiO_2	CuCl	H_2O, then H_2	375–475	2004	Törndahl et al. [94]
Ni (ALD but step 2 involves plasma)	TiN	$NiCp_2$	H_2O, then H-plasma	165	2002	Kang et al. [95]
Ni (stepwise)[a]	glass	$Ni(acac)_2$	O_3, then H_2	(1) 250, (2) 230–500	2000	Niinistö et al. [84]

[a] Stepwise metal film deposition by deposition of a metal oxide film, followed by chemical reduction of the film. Separate co-reactants and temperatures are given for each of these steps.

Atomic Layer Deposition for Transition Metal

Nitrogen-based co-reactants : Ammonia, w or w/o dihydrogen

- Key point : These reactions yield metal nitrides which decompose thermally under the reaction conditions;
  - CoN and Ni_3N decompose above 300°C.
  - Cu_3N decomposes above 200°C.
  - RuN decomposes above 100°C.

Metal precursor/co-reactant combinations that have been used for metal ALD or pulsed-CVD and employ amine or hydrazine co-reactants. This table focuses on initial literature reports for each metal precursor/co-reactant combination. The first column of the table indicates whether ALD or pulsed-CVD is claimed, although in a number of cases in Tables 1–7 ALD is claimed without demonstration of self-limiting growth.

Deposited metal (ALD or CVD)	Substrate	Metal precursor	Co-reactant	Reaction temp. (°C)	Year	Reference
Co (ALD)	H-term Si or SiO_2	$Co(amd^{iPr})_2$	NH_3	350	2010	Kim et al. [28]
Co (ALD)	H-term Si	$(allyl^{tBu})Co(CO)_3$	$N_2H_2Me_2$	140	2012	Kwon et al. [20]
Cu (decomp)[a]	glass	$Cu(PyrIm^R)_2$ (R = Me, Et)	1:1 NH_3/H_2	180	2004	Grushin et al. [112]
Cu + Cu_3N (nd)[b]	SiO_2 or Al_2O_3	$Cu(hfac)_2$	NH_3 or H_2O then NH_3	283	2006	Törndahl et al. [119]
Cu (nd)[c]	Ru	$Cu_2(amd^{sBu})_2$	NH_3	280	2006	Gordon et al. [118]
Cu (indirect)[d]	Ru	$Cu_2(amd^{sBu})_2$	NH_3 to Cu_3N film, then H_2	160, then 225	2006	Gordon et al. [118]
Cu (ALD)	SiO_2	$Cu(OCHMeCH_2NMe_2)_2$	HCO_2H, then N_2H_4	100–200	2011	Winter et al. [130]
Ni (ALD)	Si, SiO_2	$Ni(dmamb)_2$	NH_3	300	2011	Kim et al. [29]
Ni (ALD)	SiO_2	$Ni(OCHMeCH_2NMe_2)_2$	HCO_2H, then N_2H_4	175	2011	Winter et al. [130]
Ru (CVD/ALD mix)	SiO_2 or WN	$(amd^{tBu})_2Ru(CO)_2$	NH_3	200–300	2007	Gordon et al. [117]

[a] Experimental details were not provided.
[b] Not determined at this temperature, although CuN ALD was demonstrated at 247 °C.
[c] Not determined.
[d] Deposition was achieved in two separate steps (see co-reactants and reaction temperatures in the table).

Oxide Semiconductor FET for Semiconductor : Importance of ALD

Shifting from Display to Semiconductor

a-Si, LTPS, Compound Semi.
: PVD & CVD & ALD

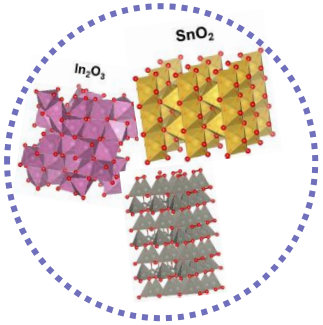
[Display]

Super-Large area display

AR/VR display

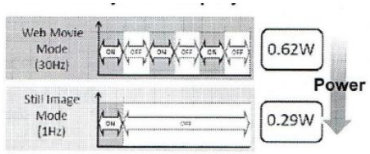
Flexible Display

○ Previous Requirement
1. Low Temperature
2. High Mobility
3. Large Area
4. Power Consumption
5. Low-Cost Process

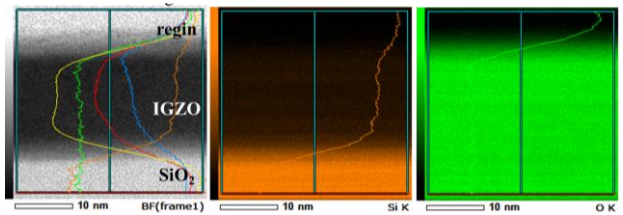


Paradigm Shift

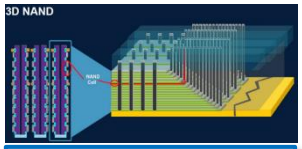
Amorphous Phase
High Mobility
Low Leakage Current
$<10^{-21}$A/um



Oxide Semiconductor TFT
+ Atomic Layer Deposition

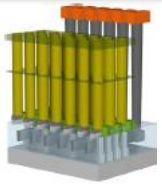


[Semiconductor]



VNAND memory

Image sensor



Dynamic RAM

○ Advanced Requirement
1. 3D Nano-Conformality
2. Low-Temperature
3. Power Consumption
4. 3D Stack Structure
5. Higher Mobility & Stability
6. CMOS Compatibility

Most Important Interests are "Low Off-Current" & Low Proc. Temp."!!!

Emerging Application: LTPO & OS-LSI

Oxide Semiconductor as a switching device – Silicon Hybrid Structure

☐ Application of OS to **Memory, Logic Device and image sensor**

… with Extremely low off-state current characteristics

: OS is stacked on a silicon CMOS circuit can open a way to evolve silicon LSI electronic devices into low-power consuming electronic devices.

■ Advantages for Oxide Semiconductor Device

1. **Low off-current Property : <10^{-24}A/um**
2. **Low Process Temperature : <350~400°C**
3. **Conventional Deposition Process: PVD & CVD & ALD**

■ Demerit for Oxide Semiconductor Device

1. **Device Performance (amorphous vs. crystallinity)**
2. **Key defects: Hydrogen, Oxygen & Ordering (crystallinity)**
3. **Process Margin (Material, Annealing (450°C, 700°C), Ambient (Hydrogen)**

Oxide FET R&D footprint for Memory Application

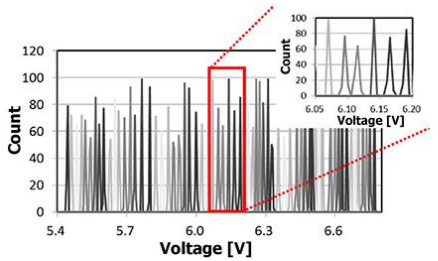
SEL (2012~Present)

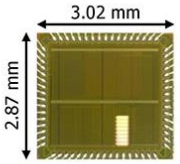
DOSRAM & NOSRAM

Low off-current

→ Long Retention

→ low power





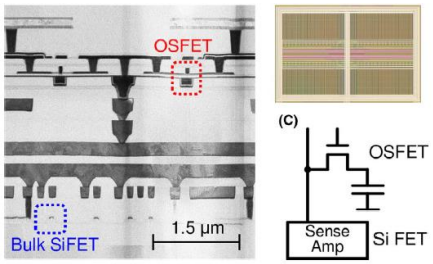
https://www.sel.co.jp/en/technology/os_lsi.html

CAAC-IGZO Review

-Various Memory Devices

- Low off-current

Less Power Consumption



YAMAZAKI, Shunpei, et al. *International Journal of Ceramic Engineering & Science*, 2019, 1.1: 6-20.

DRAM

[2012]

[2014]

[2017]

[2019]

[2020]

CAAC- IGZO DOSRAM

8kb DOSRAM

→ Low off-current

→ CAAC-IGZO FET on Si-FET

→ Data were retained after the elapse of 240 h at 85°C (around 10 days)

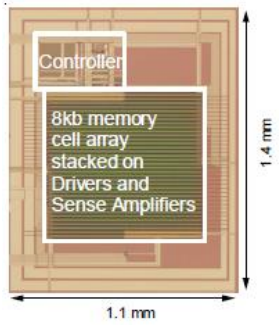
IMEC

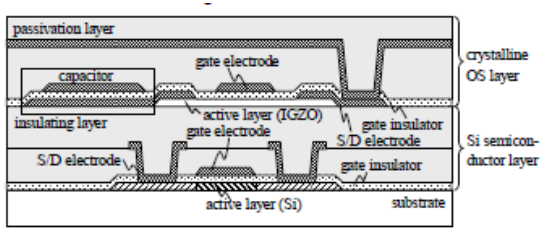
*2T0C Concept (All IGZO FETs)

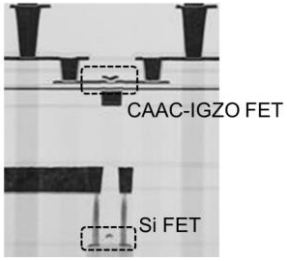
Cox of Read-Transistor as capacitor

→ M3D Memory

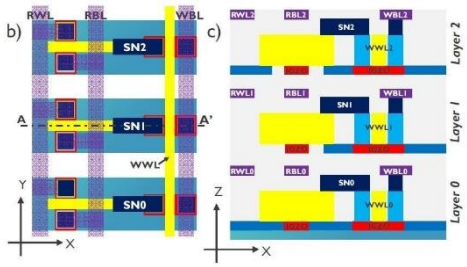
→ Increasing Density







IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 4, APRIL 2017



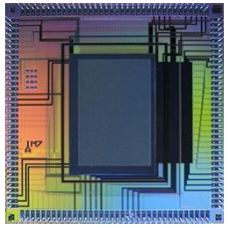
ATSUMI, Tomoaki, et al. *2012 4th IEEE International Memory Workshop*. IEEE, 2012. p. 1-4.

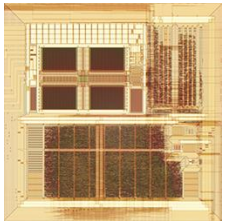
BELMONTE, A., et al. *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2020. p. 28.2. 1-28.2. 4.

Oxide FET R&D footprint for Logic Application

SEL

Image Sensor (2011)- FPGA (Field Programmable Gate Array) (2013) - 32-Bit N-off CPU (2014)



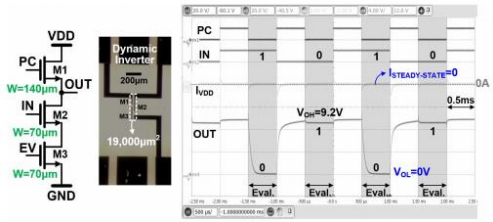


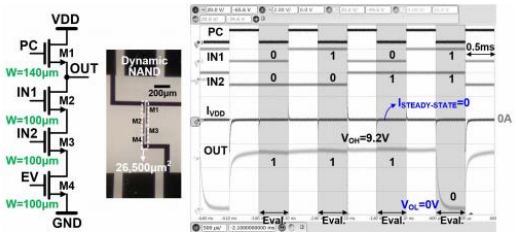
https://www.sel.co.jp/en/technology/os_lsi.html

Hanyang Univ. : Prof. Choi & Prof. Park group

Dynamic Logic Circuit based on IGZO TFTs (Scan Driver)

→ Flexible inverter, NAND





IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 10, OCTOBER 2017

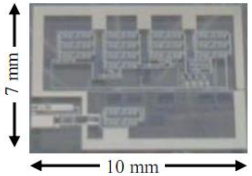
[2011] **[2011]** **[2014]** **[2015]** **[2017]** **[2020]**

Hitachi

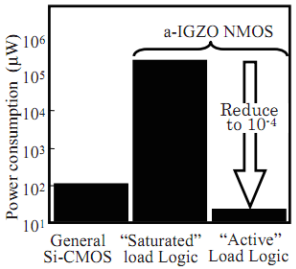
IGZO based RFID Paper

→ Low off-current

→ Low Power Consumption



Num. of Gates	351
Num. of TFTs.	1026
Power Consumption	20 μW @5 V

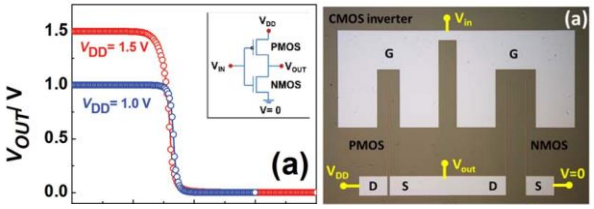


2011 Symposium on VLSI Circuits - Digest of Technical Papers, 2011, pp. 54-55.

Karlsruhe Institute of Technology (KIT)

In_2O_3/CuO CMOS Structure

→ inkjet method, Low cost

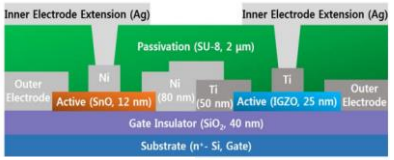


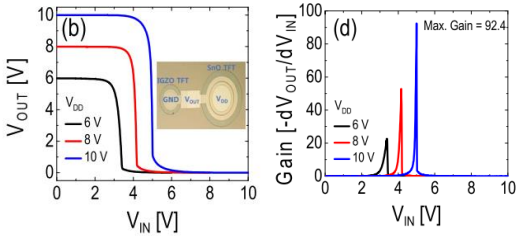
small 2015, 11, No. 29, 3591–3596

Chungang Univ.: Prof. Kwon group

IGZO/SnO corbino TFT, CMOS Structure

→ Invertor, higher gain





IEEE ELECTRON DEVICE LETTERS, VOL. 40, NO. 10, OCTOBER 2019

Recent Works in SID 2022 (1)

■ Fabrication Method for Miniaturized CAAC-OS FET for High-Definition AR/VR Displays
R. Hodo et al. Semiconductor Energy Lab, Japan, SID 2022 Digest p.310

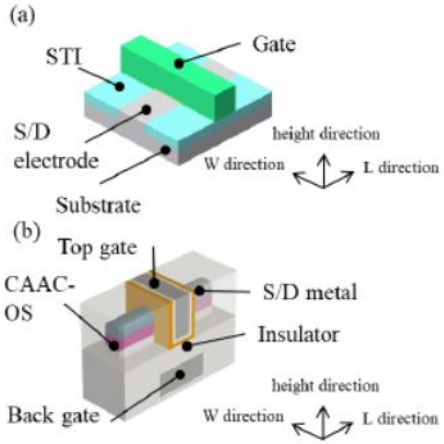
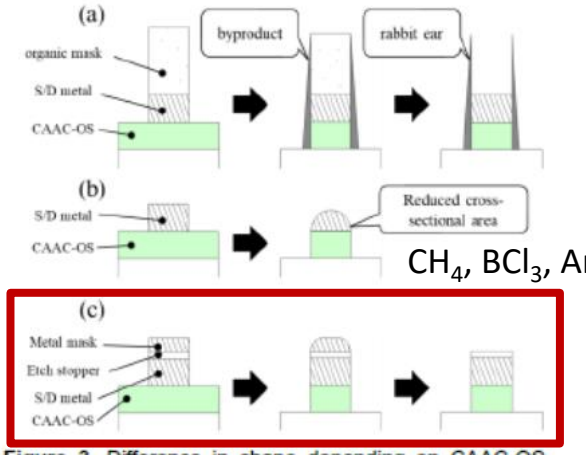


Figure 2. Bird's-eye-views of FETs
(a) Planer structure
(b) TGSA (Trench-gate-self-aligned) structure

- Back gate trench formation
- Back gate metal deposition and planarization by CMP
- Back gate insulator deposition
- **(a) CAAC-OS and S/D metal deposition and island formation**
- Insulator deposition and planarization by CMP
- **(b) Top gate trench formation**
- Top gate insulator deposition
- Top gate metal deposition and planarization by CMP
- Passivation, interlayer, via, and wiring formation

By applying a metal mask and an etch stopper, the rabbit ear and the reduced cross sectional area phenomenon that occurred in other methods was eliminated.



CH_4, BCl_3, Ar ……

Figure 3. Difference in shape depending on CAAC-OS island formation process

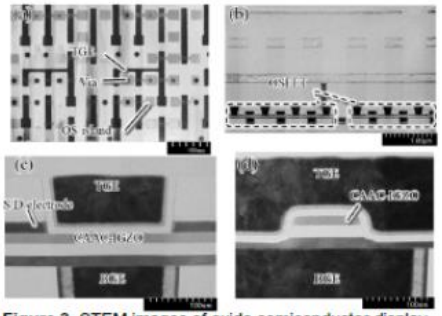


Figure 3. STEM images of oxide semiconductor display. (a) Plan-view STEM image of OSFETs. (b) Cross-sectional STEM image 1 in channel length direction. (c) Cross-sectional STEM image 2 in channel length direction. (d) Cross-sectional STEM image in channel width direction

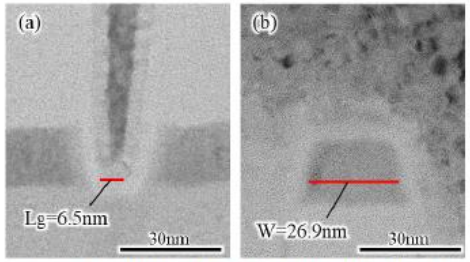


Figure 6. Crystalline CAAC-OS FET with gate length of 6.5 nm(a) cross section in channel length direction (b) cross section in channel width direction

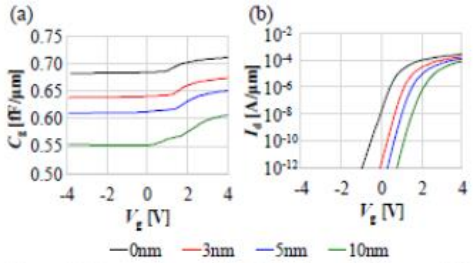


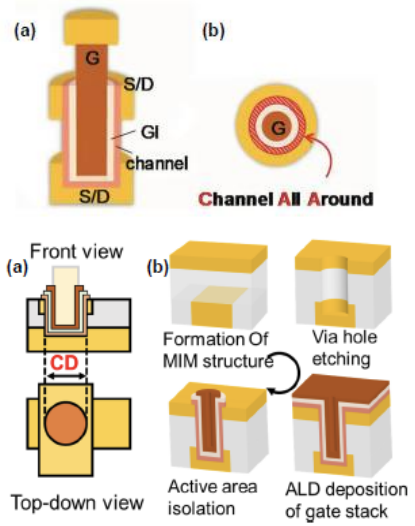
Figure 5. Comparison of (a) Cg-Vg characteristics and (b) Id-Vg characteristics between the presence and absence of different oxidation layer at ends of DE

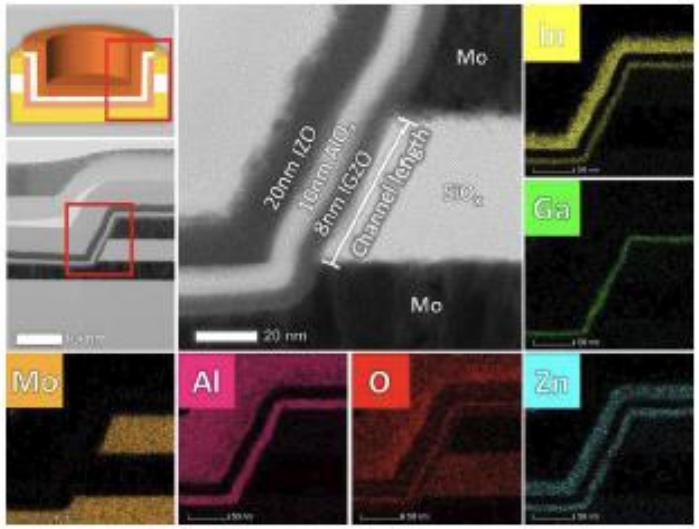
(Both of them are calculation results; C_g-V_g measurement: $V_s = V_d = V_{bg} = 0$ V, I_d-V_g measurement: $V_s = V_{bg} = 0$ V)

Y. Okazaki et al.SEL, SID 2022 Digest p310

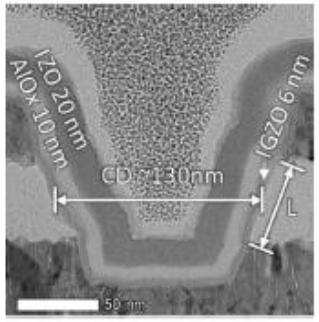
Recent Works in SID 2022 (2)

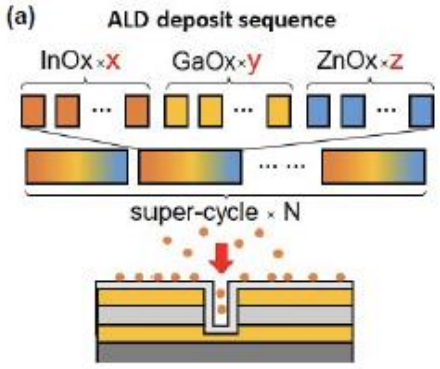
■ High-Performance Sub-50nm Channel Length 3D Monolithically Stakable Vertical IGZO TFTs for Active-Matrix Application, X. Duah et al. Chinese Academy of Science & Huawei, SID 2022 Digest p.318

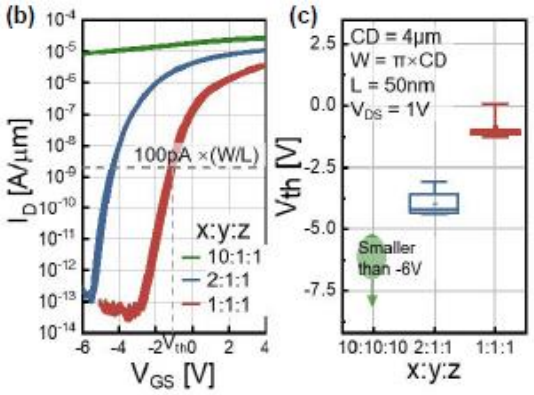


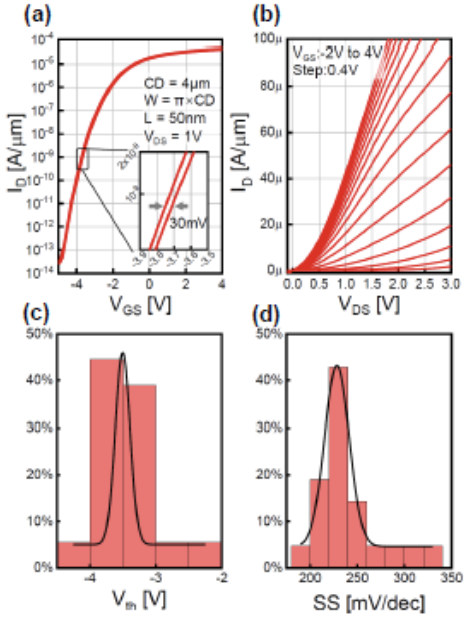


Width: π x CD, Length: Height
CD=130nm, L=50nm









Recent Works in SID 2022 (3)

■ BEOL-Compatible Ferroelectric Field-Effect Transistors with Atomic Layer Deposition of Oxide Semiconductor Channel Toward Monolithic 3D Integration, Z. Lin & Peide D. Ye (Purdue Univ.)

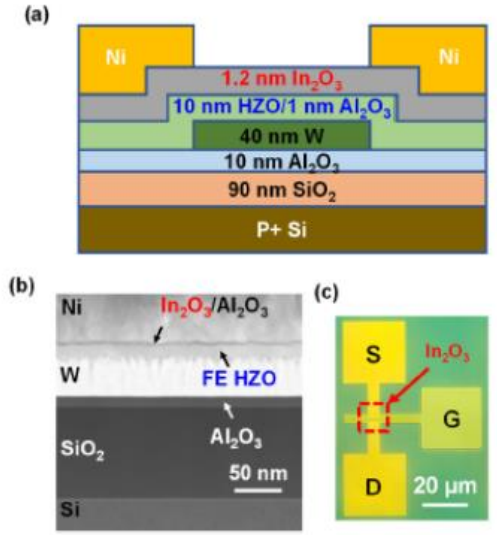


Figure 1. (a) Schematic diagram, (b) cross-sectional TEM image and (c) photo image from top view of the ALD In_2O_3 Fe-FET with W/10 nm HZO/1 nm Al_2O_3/1.2 nm In_2O_3 gate stack.

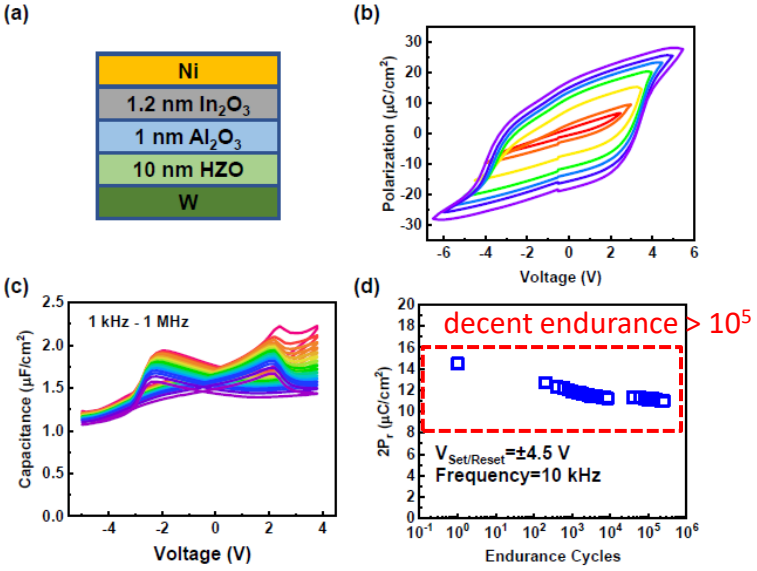
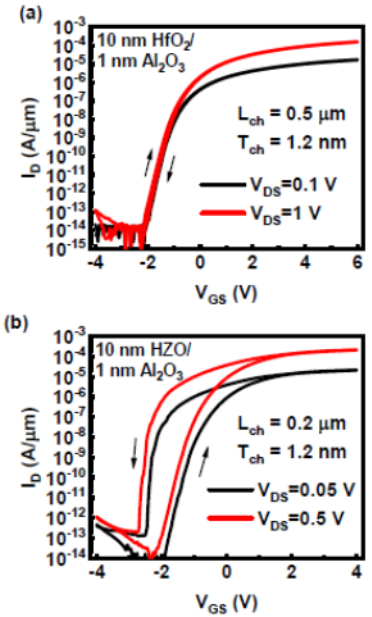


Figure 3. (a) Schematic diagram, (b) P-V, (c) C-V, and (d) endurance measurement of capacitor with W/10 nm HZO/1 nm Al_2O_3/1.2 nm In_2O_3 stack.



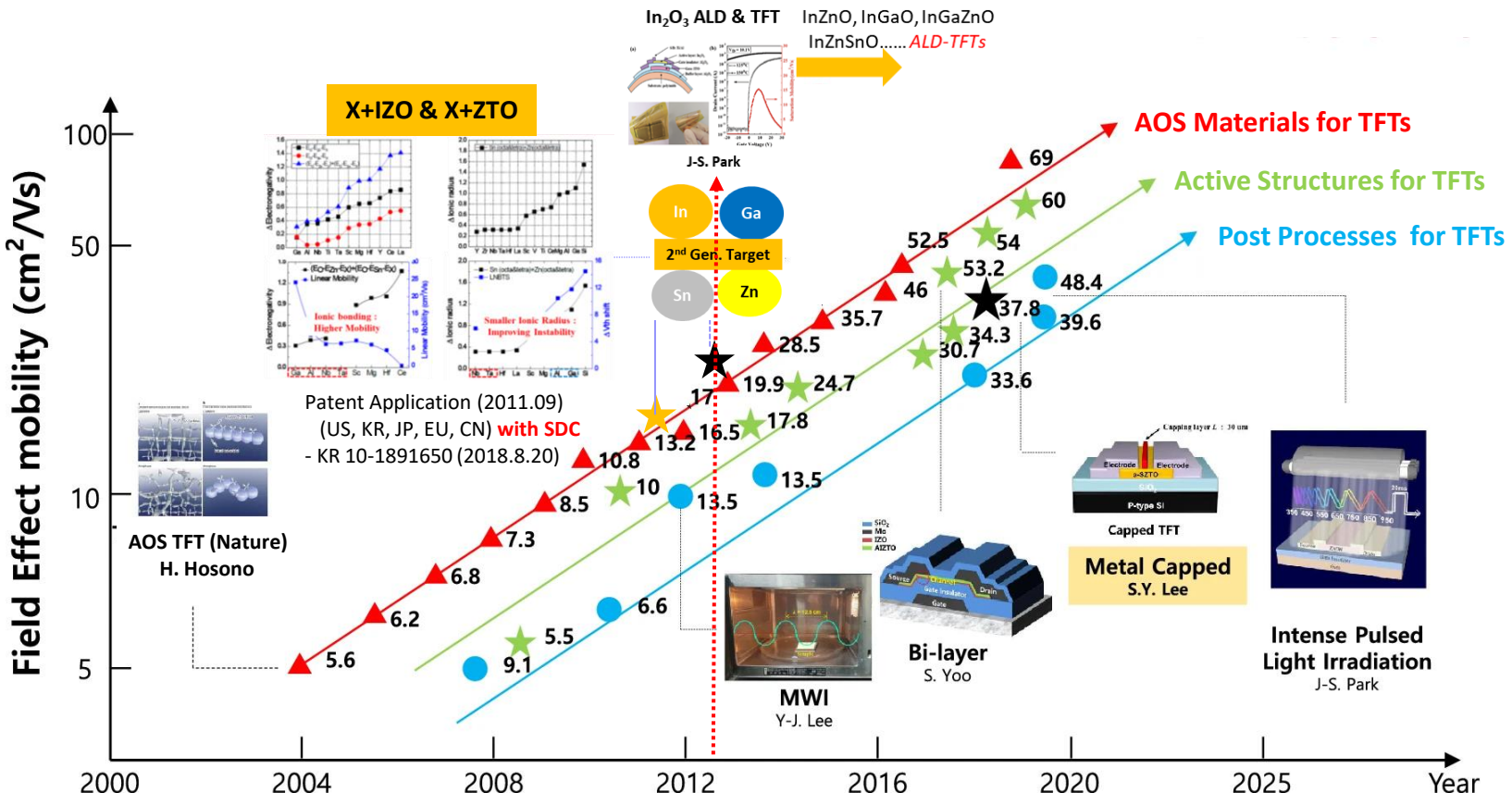
In_2O_3 ALD TFT : >100cm²/v.sec, S ~ 63.8 mV/dec
Total Thermal Budget of 400°C

Ferroelectric hysteresis loop
With a memory window of 1.2V

Recent Progress of Oxide TFT via PVD?

☐ Key Approaches for Improving *device performances* ***(Mobility & Stability)***

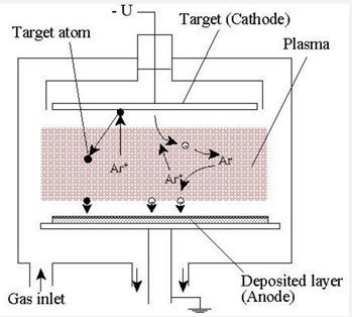
1. Combinatorial Composition : <u>Sputter Target Materials & Optimized Composition</u> (In, Ga, Zn, Sn, and so on)
2. Channel Structure via sputtering : <u>Tandem, Oxygen Scavenge</u>, and so on.
3. Post Treatment & ambient Annealing : Uniform Oxygen concentration via <u>[Energy + oxygen]</u>



ALD Values for Oxide TFTs?

■ Why is ALD Oxide Semiconductor TFT anticipated for the mass-production?

Conventional Method : Reactive Sputtering

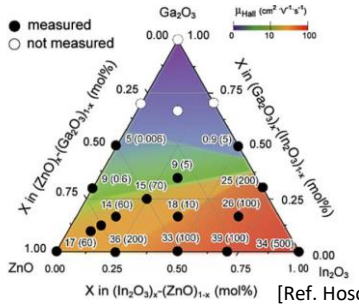


[Merits]

- Conventional Large-Size
- Well-Matured Thin Film Tech.
- Conductive IGZO Target

  Reactive DC sputtering .

[Demerits & Limits]



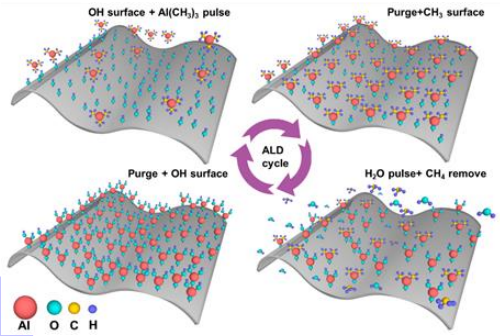
[Ref. Hosono Group]

- Conventional Thickness
  : Below 20~30nm thick
- Ternary Oxide System
  : InGaZnO
- Oxygen Ratio & Annealing

- Uniformity of Composition & Thickness
  → SRU &LRU of Device Performance on Large Area
- Difficulty of in-situ Cation's combination
  → In-situ Insulator, improving mobility & reliability

Promising Tool: Atomic Layer Deposition

[Limits]



- Low Throughput Issue
- Proper Precursors (In..) & Chemical Reactions
- Large Size Equipment

Now, On going to Mass-Production!

[ALD Merits]

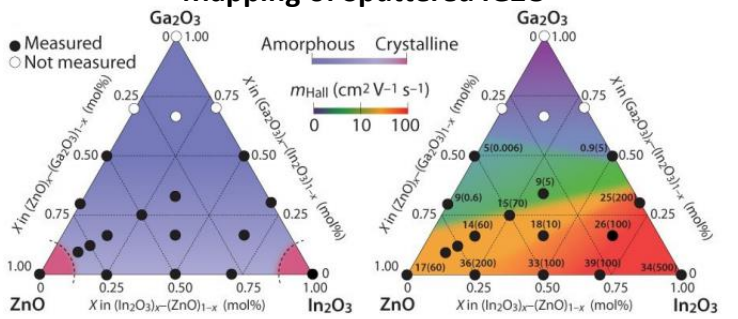
1. Beyond Sputtering method
   : Reliability & Repeatability
   : In-situ multi-composition
   : Nano-level controllability even in 30nm thick
2. Nano-Control : Thickness & Composition
   Even on very large-size substrate (>8G)
   : Excellent Uniformity on both thickness & composition

Atomic Layer Processing for Oxide Semiconductor TFT

I. *in-situ* Combinatorial Composition

Previous Mapping Diagram of Sputtered vs PEALD InGaZnO

< Mapping of Sputtered IGZO>

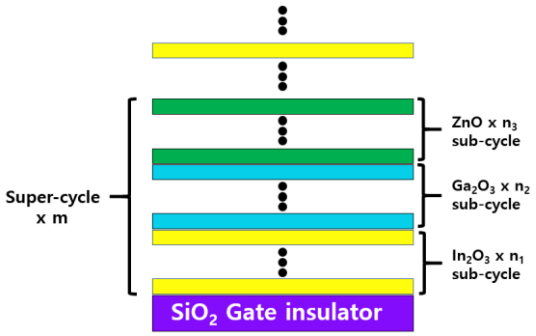


NPG Asia Mater. 2, 15 (2010)

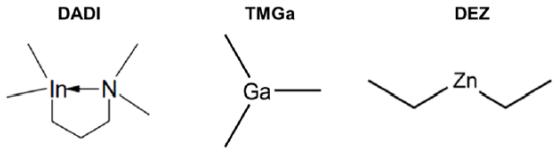
- Micro-structures:
  - In, Zn↑ : amorphous → crystalline
- Electrical property:
  - In, Zn↑ : Hall mobility ↑
    : Hall carrier concentration ↑

→ Obtaining mapping data from PEALD IGZO is essential, valuable, and very easy.

< ALD Sequence >



< PEALD Experimental information >



- **Deposition method: PEALD**
- **Reactant: O_2 plasma**
- **Growth Temp.: 200°C**

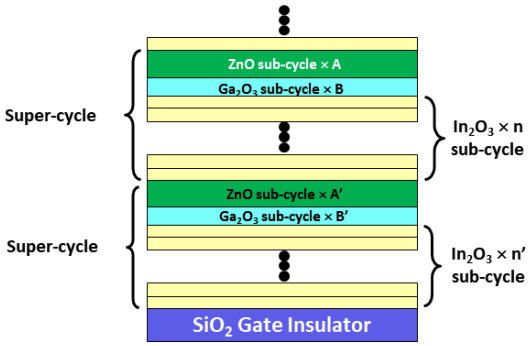
In_2O_3	Ga_2O_3	ZnO
0.8 (A/cycle)	1.2 (A/cycle)	2.2 (A/cycle)

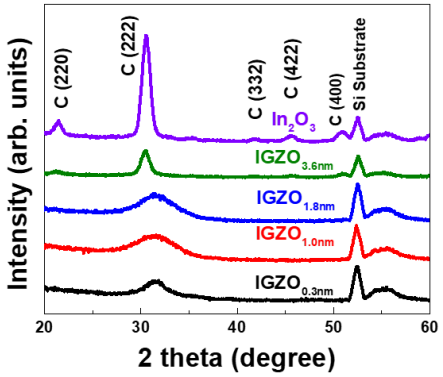
Sheng et al. ACS Appl. Mater. Interfaces 11, 40300–40309 (2019)

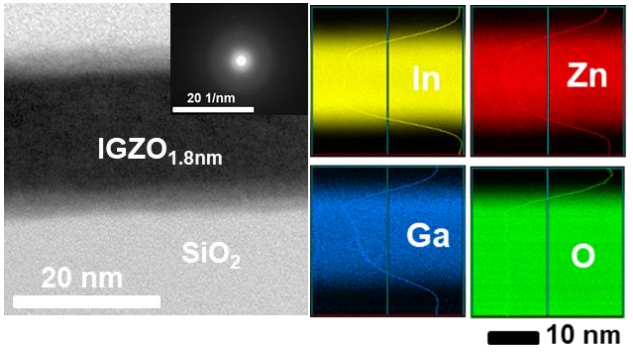
Atomic Layer Processing for Oxide Semiconductor TFT

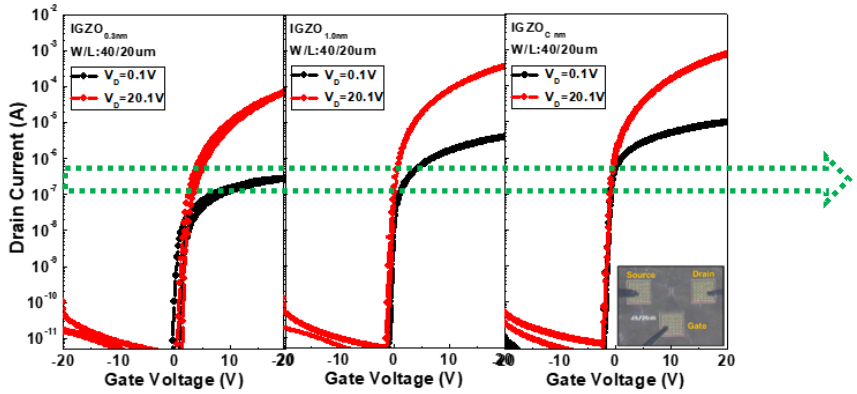
I. *in-situ* Combinatorial Composition

☐ High mobility of PEALD InGaZnO TFTs : In-rich phase









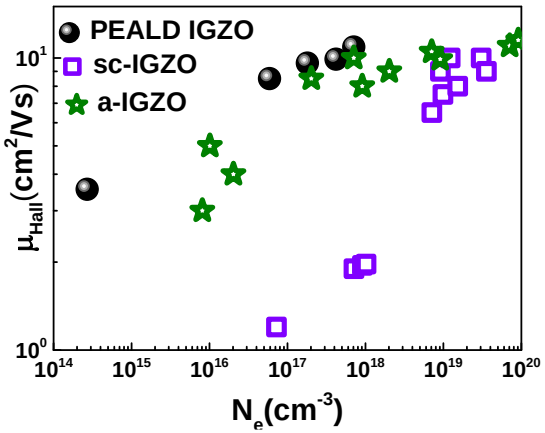
	$IGZO_{A\ nm}$	$IGZO_{B\ nm}$	$IGZO_{C\ nm}$
V_{th} [V]	2.3±0.3	0.2±0.1	-1.3±0.1
μ_{eff}[cm^2/Vs]	4.8±0.2	30.3±0.8	**65.5±1.2**
μ_{sat}[cm^2/Vs]	9.9±0.1	34.1±0.3	**74.3±1.5**
S.S. [V/decade]	0.34±0.03	0.26±0.02	**0.26±0.02**
Hysteresis [V]	0.56±0.1	0.20±0.04	**0.20±0.03**
I_{ON}/I_{OFF}	2.9×10^8	5.5×10^8	8.9×10^8

Sheng et al. ACS Appl. Mater. Interfaces 11, 40300–40309 (2019)

Atomic Layer Processing for Oxide Semiconductor TFT

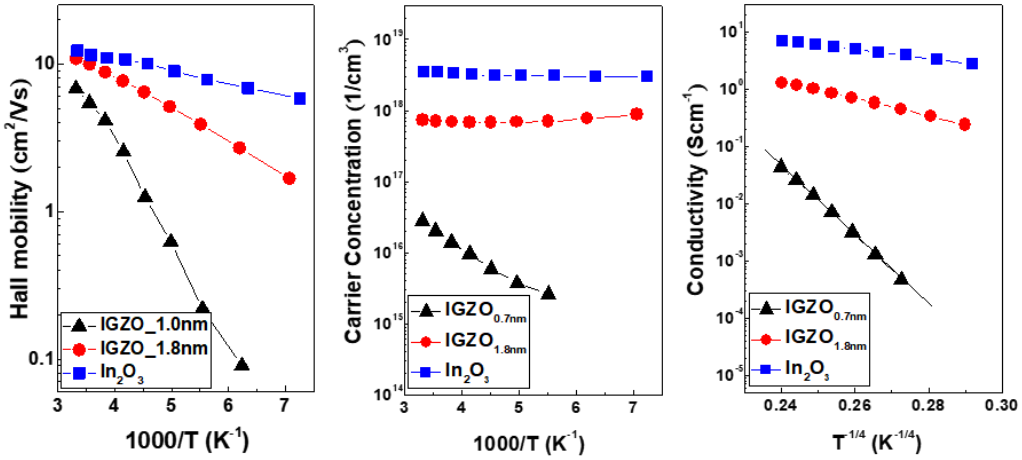
I. *in-situ* Combinatorial Composition

Hall mobility & N_e (RT)



- In_2O_3 sub-cycle number increase
  → carrier concentration↑
- Dependency of μ_{hall} and N_e
  → Similar trend to sc-IGZO and a-IGZO
- At Same N_e
  → μ_{hall}:PEALD IGZO ~ a-IGZO > sc-IGZO

Low temperature Hall measurement



- IGZO < 1.0nm → N_e (< 10^{17} cm^{-3})
  : E_F locate in tail states & carrier conduction limited by potential barriers
  → temperature-dependent behavior
- IGZO > 1.0nm → N_e (> 10^{17} cm^{-3})
  → Fermi level exceeds the potential barriers
  → carrier transport is no longer affected by the potential barrier
  → temperature independence

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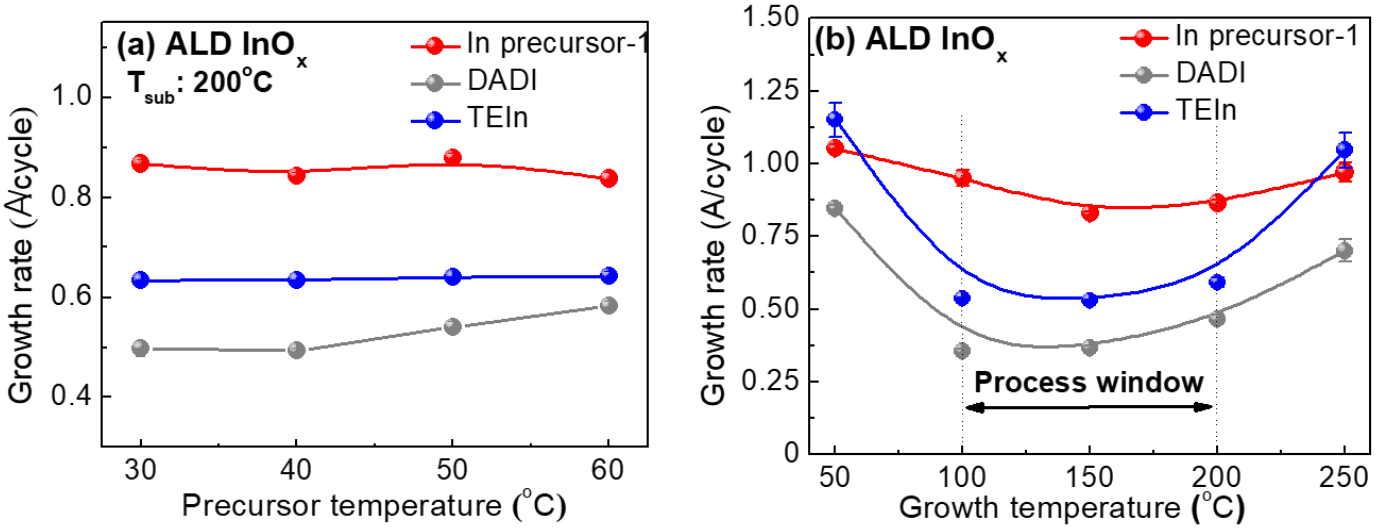
Atomic Layer Processing for Oxide Semiconductor TFT

II. Surface & Chemical Reaction

☐ Dependency of each In precursor for In_2O_3 ALD

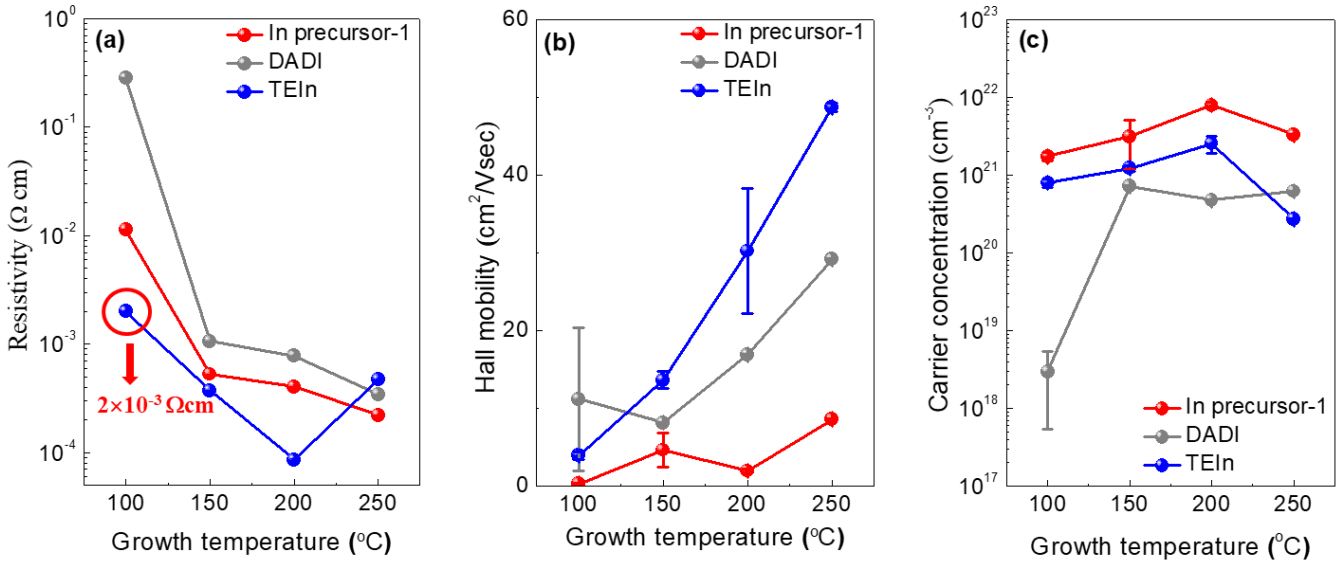


- All Indium precursor exhibited self-limiting Behaviors under ozone reactants.
- They have similar ALD process windows Between 100 and 200°C. No thermal-decomposition below 250°C.

Atomic Layer Processing for Oxide Semiconductor TFT

II. Surface & Chemical Reaction

☐ Dependency of each In precursor for In_2O_3 ALD



■ InOx film with TEIn exhibited low resistivity (below ~10^{-4} Ωcm) over 150°C.

■ In general, Hall mobility increased linearly on growth temperature due to the crystallinity. Most films have high concentrations on all growth temperatures.

Atomic Layer Processing for Oxide Semiconductor TFT

Mother Matrix

ZnO ALD

Low Mobility due to G. B.
Limited Device Stability

Group III doped ZnO ALD
Still Low Mobility (1~3cm²/V.sec)
: G. B. & Al-O effect

ZnSnO ALD
Moderate Mobility (10~15cm²/V.sec)
: Limitation of Sn conc. due to Etch

ZnSnO based Oxide TFT
1. Stable SnO_2 phase; Etch?
2. X-ZTO system
3. High mob. & Stability (>20cm²/V.sec)

Mother Matrix

In_2O_3 ALD

: How to control Vo?
Non-stoichiometry O/In?

J. Sheng et al. ACS AMI 11, 12683 (2019)
J. Sheng et al. J. Semicond. 39 011008 (2018)
W. Choi et al. JVST A 37 020924 (2019)
M. Kim et al. Ceramics International (2019)
J. Lee et al. ACS AMI 10, 33335 (2018)

InGaOx ALD
Reasonable Mobility(>15cm²/V.sec)
Necessary for the Optimization
Ga, In Precursor & ALD Process

Understanding Combination!!

InZnOx ALD
Better Mobility(>40cm²/V.sec)
Good Stability on TG or BG PA?
In Precursor & ALD Process

InGaZnO ALD
Good mob. & Stab. (>40cm²/V.sec)
Necessary for the Optimization
Ga, In Precursor & TG/BG PA

InZnSnO ALD
Good mob. & Stab. (>30cm²/V.sec)
Necessary for the Optimization
In, Sn Precursor & TG/BG PA

Better Mobility & Stability !!

There are a lot of possibilities using ALD methods for designing oxide Material & TFTs

Summary

1. ALD is well-known thin-film technique, but the chemistry is the fundamental in ALD.
2. The challenges of ASD are significant. However, it is an interesting area, fundamental research in academia and industry.
3. MLD is getting important for novel function and property
4. Ru and Mo ALD is the key for next generation. The reducing agent is one of key technologies in metal ALD for next generation.
5. It is inevitable to design 3D structure for increasing the density.

   Currently, new semiconductor is very critical issue for 3D Memory devices.

   : ALD is the key process in Semiconductor industry.

   Providing Not only conformal deposition in 3D structure but also New Breakthrough!

Thanks for your attentions!

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Lab: http://hylime.kr